

Capabilities Tour

Welcome to the Cleverscope Capabilities Tour

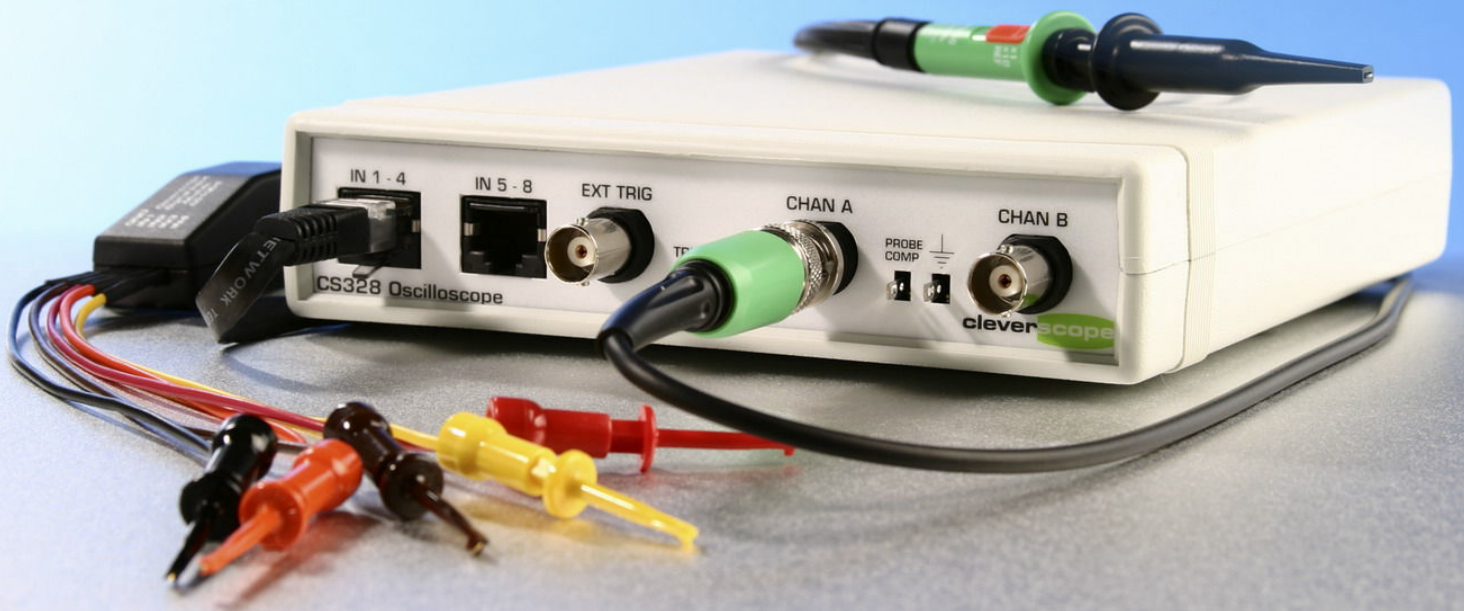
This resource discusses Cleverscope capabilities using common applications to illustrate each capability.

Cleverscope Oscilloscope capabilities.....	2
Stepper motor control.....	2
Custom Units.....	3
Zooming Tracking Graph.....	4
Using Maths to extract signal information.....	5
Maths processed response.....	6
Dual Trigger Capture.....	7
CCD control.....	9
Dynamic Range optimised scale and offset.....	9
Count based triggering.....	10
Filter Response Evaluation.....	13
Spectrum Display and Signal Generator Control.....	13
Comparison with other oscilloscopes.....	15

Cleverscope is an integrated tool with these capabilities:

- Oscilloscope with comprehensive trigger facilities
- Mixed signal Analog + Digital capture and display
- Spectrum Analysis to examine spectra and transfer response
- Signal generator to excite equipment being tested.
- Mathematics module to extract valuable signal information

This is a general discussion. For further, detailed information, see the Cleverscope Guided Tour, Triggering Tour, Screen Shots, Application Brief, Competitive Comparison and Datasheet documents at www.cleverscope.com/resources/



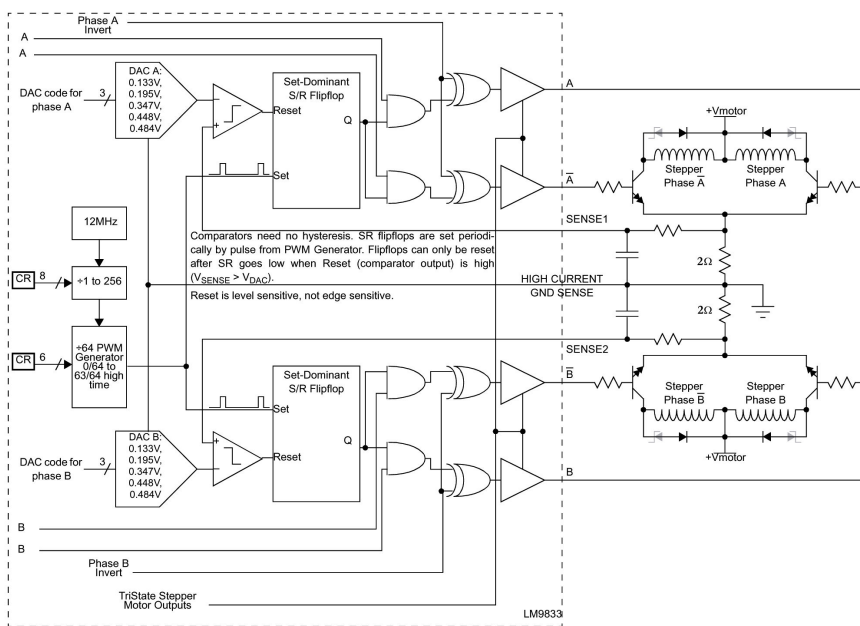
Cleverscope Oscilloscope capabilities

We will use the design and implementation of a National Semiconductor LM9833 based USB connected scanner as a measurement example. The LM9833 integrates USB, CCD scanner interface, stepper motor control, user interface and pixel data storage and transfer into one chip. We will examine parts of the Scanner design process using Cleverscope.

Stepper motor control

The stepper motor is used to transport the scanning head past the paper, in a flatbed scanner. We wish to verify that the stepper motor control system is working properly.

Here is a block diagram of the LM9833 stepper motor control section. A two phase centre tapped stepper motor is used, with micro-stepping to achieve $\frac{1}{4}$ full step resolution. PWM is used to achieve the $\frac{1}{4}$ step. The phase outputs are A and A* and B and B*. Closed loop control of the current in the stepper motor is achieved by feeding back the voltage across the two $2\ \Omega$ current sense resistors (labelled Sense 1 and Sense 2).



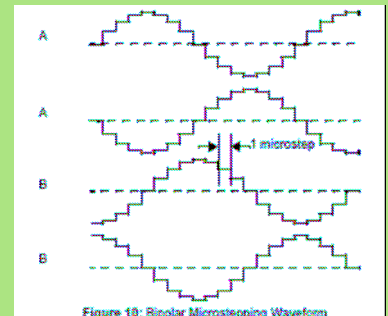
Using Cleverscope we can investigate the performance of the PWM control system.

Stepper motor PWM control

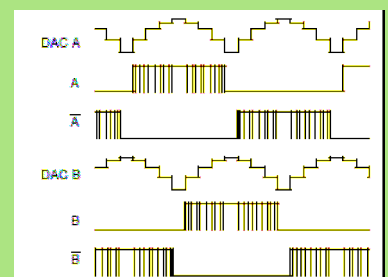
The stepper motor uses a wound stator, with a large number (typically 100) pole pairs distributed around the stator. Two windings are used; the first winding is wound onto the first pole of the pole pair, and then onto the first pole of the next pole pair and so on. The other winding is wound onto the second pole of the pair, and then onto the second pole of the next pair and so on. The windings thus alternate poles all the way around the stator. The motor controller works by exciting first one winding and then the other winding, which causes the rotor magnetic flux vector to step from one pole to the next. This process is repeated to rotate the motor.

A further refinement is to use an effectively sinusoidal variation of current in the motor windings, rather than the square wave current used in the simple case. Sinusoidal variation of the current allows finer control of the magnetic flux vector (which is essentially the phase difference between the two winding currents). This is called micro-stepping. To improve efficiency, the sinusoidal current is approximated by a PWM sequence which uses the motors rotor inertia to mechanically filter the PWM.

Here is the required current:



And here are the resultant PWM winding signals:



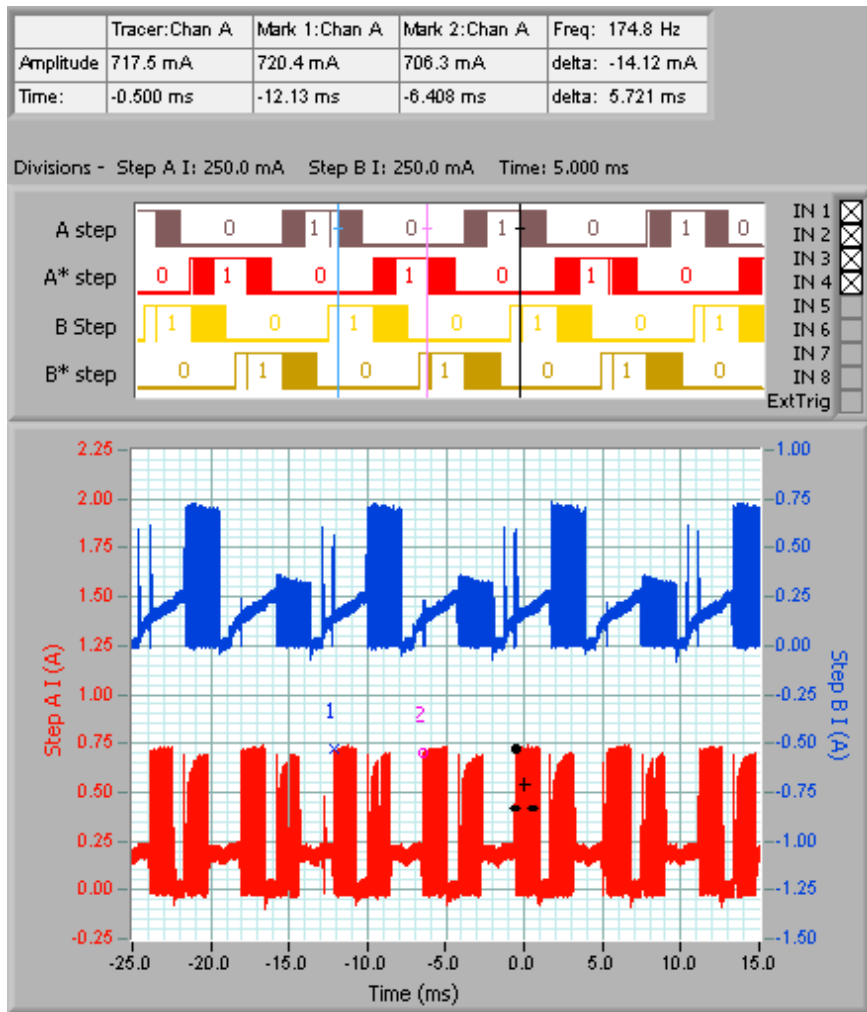
Note that feedback will change the PWM signal to maintain a sinusoidal current, and this may add additional pulses.

Custom Units

Our first task is to capture a signal. We set up the Cleverscope as follows:

- Chan A – Across Winding A 2 Ω Current sense resistor.
- Chan B – Across Winding B 2 Ω Current sense resistor.
- Digital Input 1 – Step A
- Digital Input 2 – Step A*
- Digital Input 3 – Step B
- Digital Input 4 – Step B*

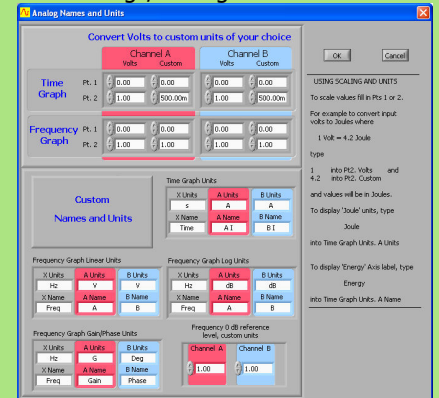
It's easier to understand the graphs if they are usefully labelled. So we label using the Settings/Analog Names and Units, and Settings/Digital Names and Colours menu items, as shown in the sidebar. We start the stepper motor running, and capture:



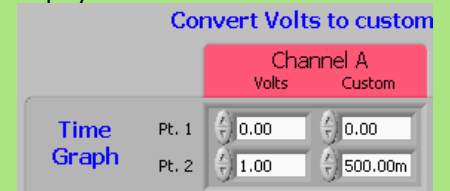
We have captured around 4 steps. Notice the graph shows a peak current of about 720 mA, with a step frequency of about 175Hz.

Custom Units setup

Use Settings/Analog Names and Units...



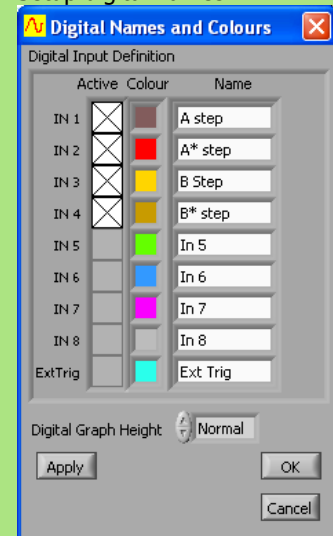
Because a 2ohm current sense resistor is used, each 1V in equates to 0.5A displayed:



Setup analog names:



Setup digital names:



Zooming Tracking Graph

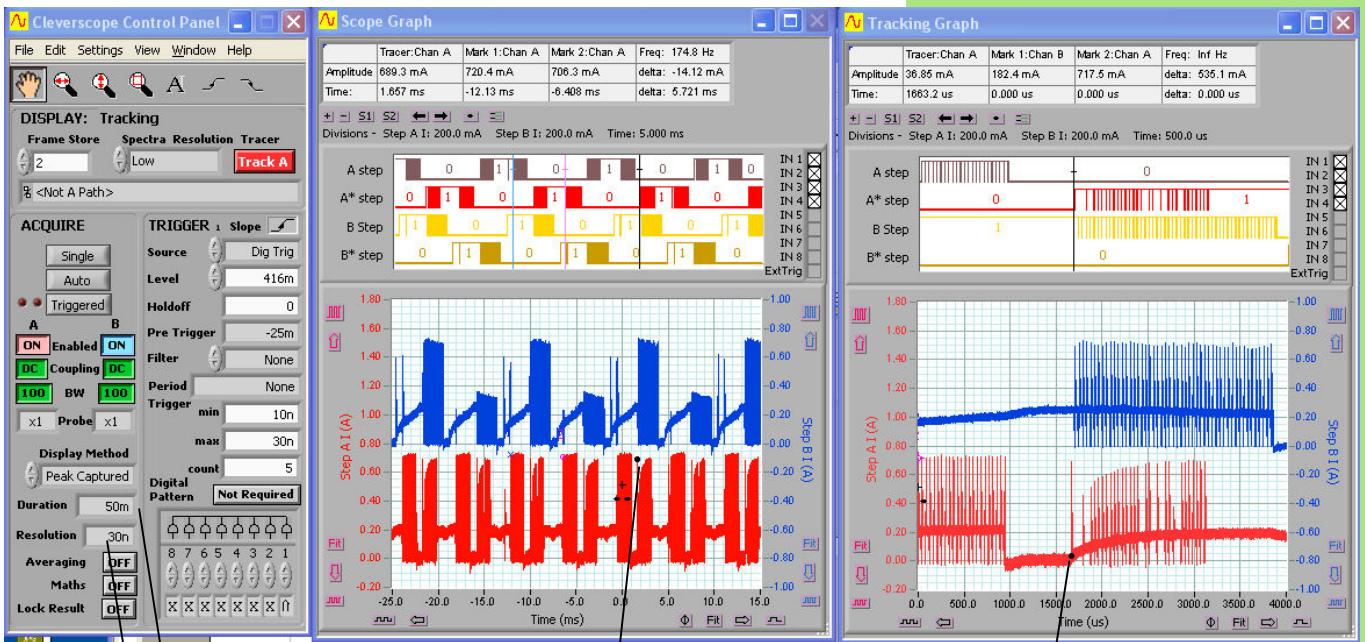
Once captured we can zoom on the signal, to check out signal statistics. We use the Tracking graph to do this. A screen shot is shown below. The Cleverscope Control Panel is used to set up the Trigger and capture settings. The scope graph sets the time and amplitude definition for the Cleverscope Acquisition Unit (CAU). The tracking graph is used to examine the signal in detail

Notice that we are triggering off a Digital trigger , in this case Input 1 (A step) rising. More sophisticated triggers will be discussed below.

Scope graph setup

The CAU capture specification is set to match the Scope Graph. The CAU captures signal from 1 division before the left hand edge of the scope graph (in this case – 30ms) to 1 division after the right hand edge (in this case 20 ms). The total duration is 50 ms.

The A channel digitises signals in the range –0.2V to +1.8V. The B channel digitises signals in the range –1 to +1V. The CAU automatically scales and offsets the signal to present the full range specified by the scope graph setup to the Analog to Digital Converter.



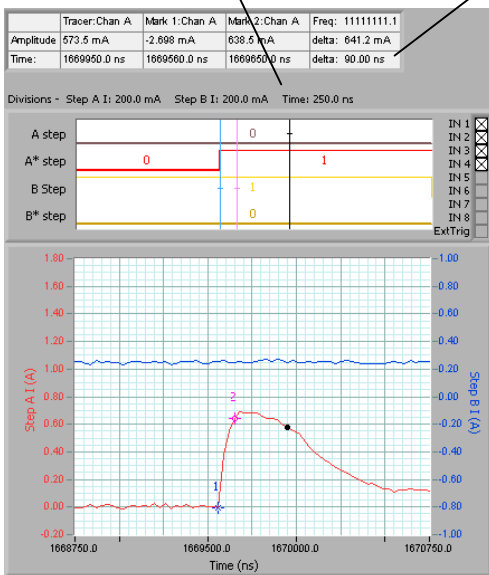
50ms duration
30 ns resolution

The current tracer position, and the tracking graph centre.

The tracking graph tracer is mirrored to the scope graph

Graph division values

90ns delta



We can zoom all the way in to the limits of the current resolution (in this case 30ns) anywhere on the scope graph. Here we zoom on the single pulse shown in the tracking graph above.

Notice the time per division is 250ns, there is still a long way we can zoom.

We also see the rise time is 90 ns, and the amplitude 680 mA.

CAU sample memory

The CAU has 4M samples of memory. Each sample is composed of 2 Analog + 8 digital + Ext Trigger values.

The sample memory is partitioned into **frames**. With the minimum 2 frames, each frame has 2M samples content. This means you can capture up to 20ms and still retain 10ns resolution. Once we go above 20 ms, the resolution is reduced. With 50ms capture time our resolution is $50\text{ms}/2000000 = 25$ ns. This is rounded up to the nearest 10ns interval, which is 30ns.

You can capture more frames, and use them as history, or for averaging, but time resolution will reduce.

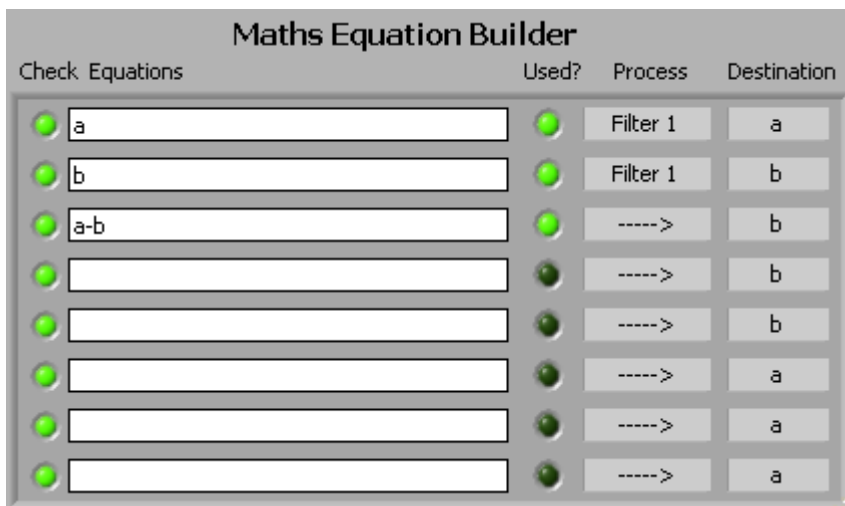
Using Maths to extract signal information.

The stepper motors are excited with PWM signals designed to generate a sinusoidal motor current. There are two reasons for this; to increase the step resolution, and to reduce noise. We can use Cleverscope's Maths capability to filter the motor current signal to approximate the mechanical torque the motor sees.

Firstly we use View/Maths Equation Builder to show the Maths module, and we setup a filter to approximate the motors rotor time constant, in series with the driving resistance/motor inductance. We find from the manufacturers data, that the time constant is 630us. We can approximate the motor (+ series LR) as a 4th order low pass filter, with a corner frequency of approx $1/(2\pi\tau)$ where τ is the rotor + series LR time constant. We find the corner frequency to be about 252 Hz.

Secondly, we are interested in the vector generated as a result of the difference between the A and B winding currents. In the example below, we have set $B = A - B$, which calculates the difference in the filtered winding currents. This value is proportional to the step torque.

Here is the Maths Equation Builder setup:



Only equations for which Used? Is selected are processed. Here we Filter A and B, and then subtract B from A and output that to B.

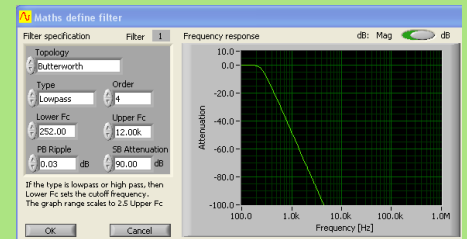
The result of each line is fed to the next line as inputs. This means the a-b calculation evaluates the filtered versions of Channels A and B.

Filtering

We have used Filter 1 to filter both the A and B channel waveforms.

We calculated the corner frequency for our low pass filter as 252 Hz.

Here is the Filter Setup, showing the amplitude response:



Two filters are provided, and you can interactively design a filter to suit your requirements.

The Maths Equation builder is used to build up to 8 sequential Maths equations. The results of one line are fed in as the inputs to the next line.

You can write equations using Channels A-D (C and D maybe used as holding channels) and I1-I8 and ET.

The equations are any combination of inputs and operators and functions.

For example you can write an equation such as

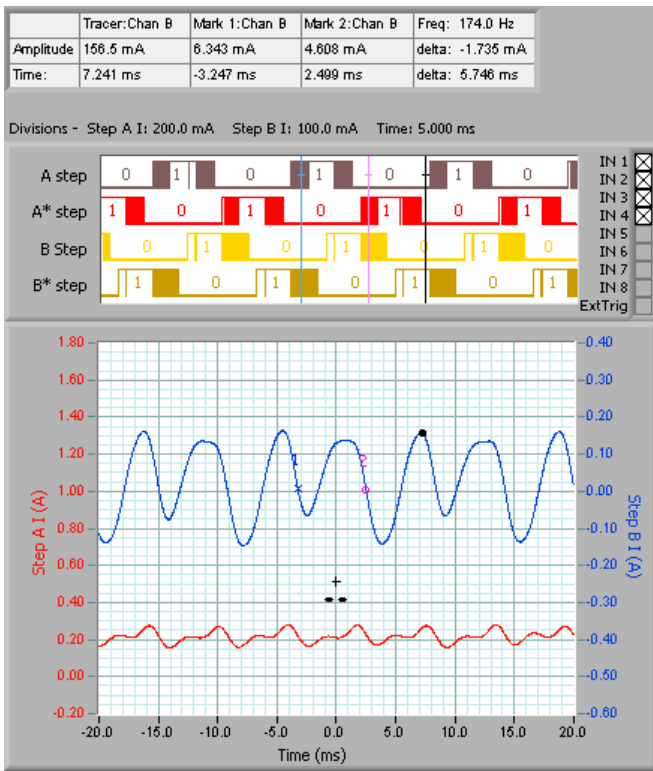
$$\text{Sign}((20 * (\log(a) - \log(b)) - 36)) \text{ ---> In 1}$$

Which will find the dB difference between A and B, subtract 36 from it, and then put 1 into In 1 if the result is positive, or 0 if it is not – ie, it tests if the dB difference between A and B is greater than 36 dB.

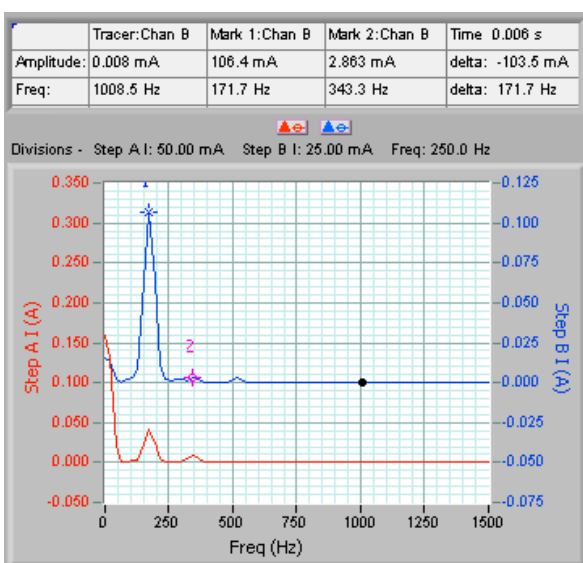
The entire channel can be processed before it is output. Processes are a transfer (--->), Integral, Differential, and Filter.

Maths processed response

Channel B shows an approximate sinusoidal motor torque. Channel A shows the filtered motor current for the A winding.



The step frequency is about 174 Hz. Distortion in the motor torque generates noise, and increased heating. We can estimate the torque current by looking at the spectrum graph:



We see the effective torque current is about 106 mA, with a step frequency of 172 Hz. The harmonics will contribute to noise and reduced smoothness. At this point we can verify the average motor current, and step frequency are correct to the design.

Design Verification and Synthesis

The Maths module is useful to do both design verification, as we have done here, but also design synthesis.

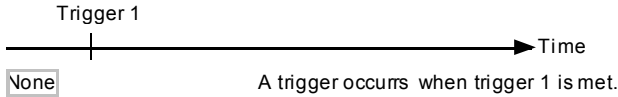
The Cleverscope can be used to capture signals that will be used as the input to some processing system. The Maths module can then be used to model the processing system, and the outputs displayed directly on the graph. The user can verify they are as expected, and if not, iterate the process.

When the real process has been built, outputs from it can be captured (with the Cleverscope), and compared to the previously modelled outputs to verify the process design.

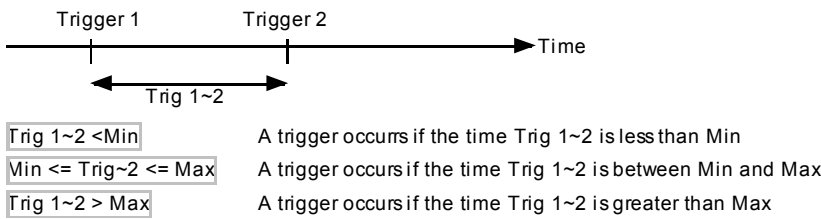
Dual Trigger Capture

Cleverscope provides two sequenced mixed signal trigger definitions. You can trigger on the following conditions:

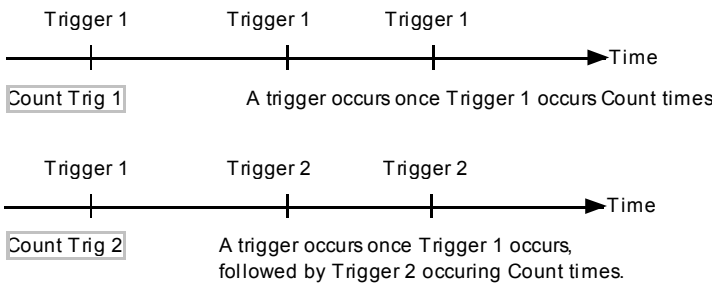
Edge or State Trigger



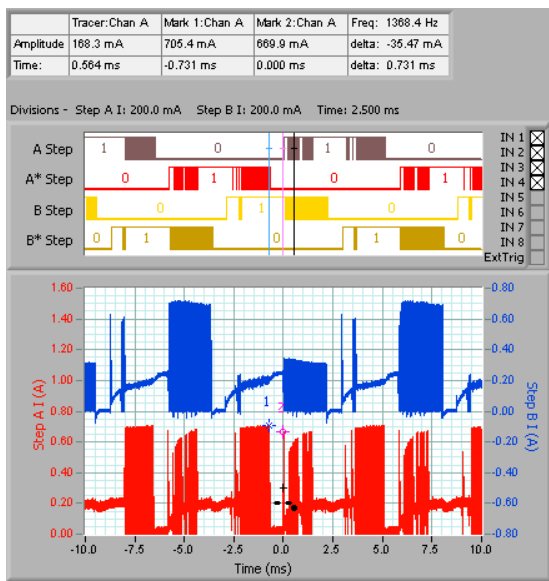
Duration Triggers



Count Triggers



The count can vary from 1 to 2.147×10^9 , while the time can vary from 10ns to 42.9 seconds.



the start of the step.

In our stepper motor example, we triggered arbitrarily on a Step A digital input. However we might prefer to trigger at the beginning of a step. Notice from the graph that the start of A step follows the end of A* Step with a period of about 730us – the gap between Markers 1 and 2 in the graph.

We can use a time duration trigger where a falling edge through 0.4A is followed by a rising edge through 0.4 A at least 730us later to find

Trigger Definition

Each trigger definition specifies the source (Chan A, Chan B, External Trigger or Digital Inputs), the trigger level (if analog), and a digital pattern.

For digital triggering you can specify rising, falling, high level, low level, or don't care for each input. You can AND or OR bits to create a complete digital definition.

As an example here we look for a rising edge (with noise filtering) on Chan A at 200m, with the digital inputs required to be In 4..1 = 1010, followed by a digital trigger with either (Input 1 rising OR Input 2 falling) AND inputs 5..3 = 001, and further only trigger if these events occur within 20 to 60ns of each other.

TRIGGER 1 Slope

Source Chan A

Level 200m

Holdoff 0

Pre Trigger 1.5m

Filter Noise

Period Trig 1~2 < min

Trig 1~2

min 20n

max 60n

count 5

Digital Pattern Required

Trigger 2 definition Slope

Source Dig Trig

Level -100m

Digital Pattern Not Required

8 7 6 5 4 3 2 1

8 7 6 5 4 3 2 1

8 7 6 5 4 3 2 1

The external trigger and digital input thresholds are set using the

Settings/Acquisition Settings... menu. Here, for example, we have the external trigger threshold at 0V, and the digital threshold at 2V.

Acquisition settings

Threshold voltages

External Trigger (V)

2.5 5.0 7.5 10.0 12.5 15.0 18.0

0.0 -2.5

0.00

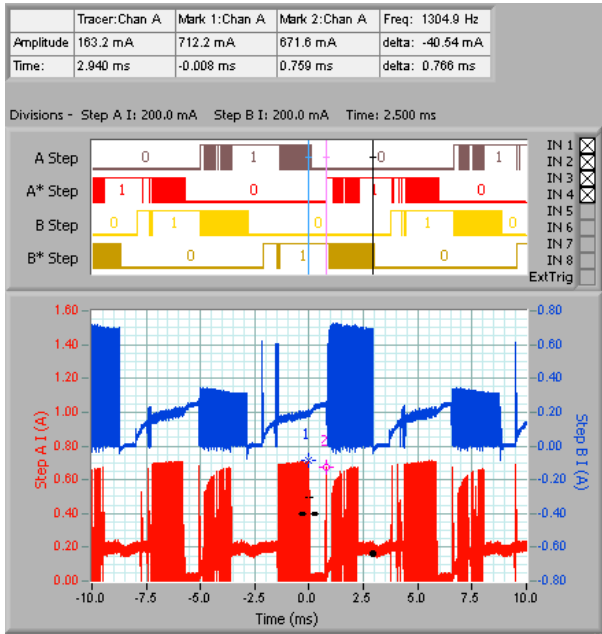
Digital Inputs (V)

4 5 6 7 8 9 10

2 3

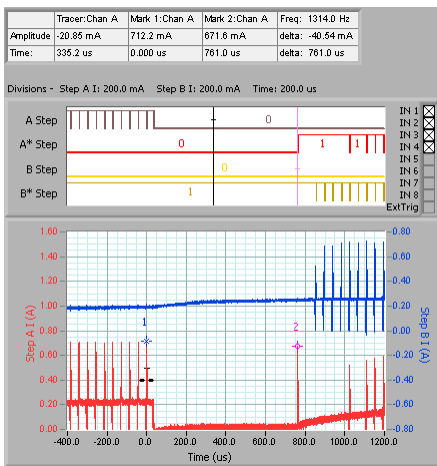
2.00

Here we see the results with this simple version of the dual trigger:

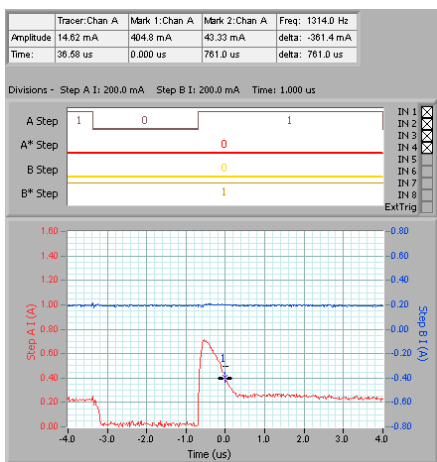


The trigger is located at the point which meets the trigger specification. In this case the duration 1~2 is 766us.

We can zoom in further to see the actual trigger point, as shown in the view below.



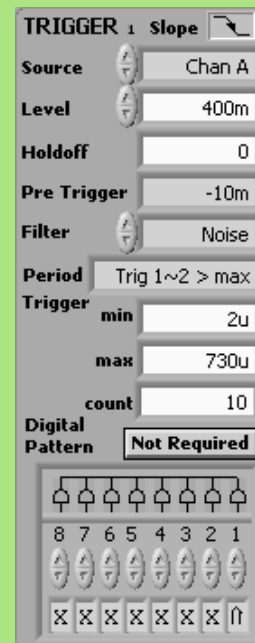
The zoomed in view shows the required duration between the pulses. Marker 1 shows the trigger location.



Zooming in further on Marker 1 shows that we triggered at the correct amplitude of 400 mA.

Notice in the expansion that the digital channel A Step actually had a pulse just before the trigger that is not easily seen in the zoomed out view.

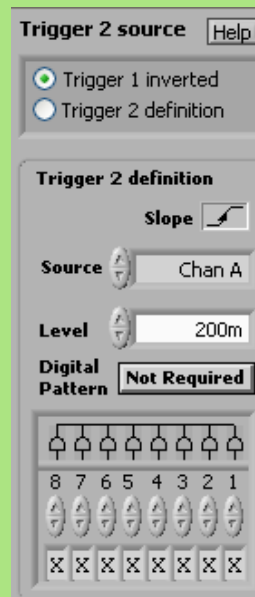
Duration Trigger Example



Trigger 1 fires if Chan A falls through 400mA.

A period trigger, with Trig 1~2 greater than 730us has been specified.

A digital pattern is not required.



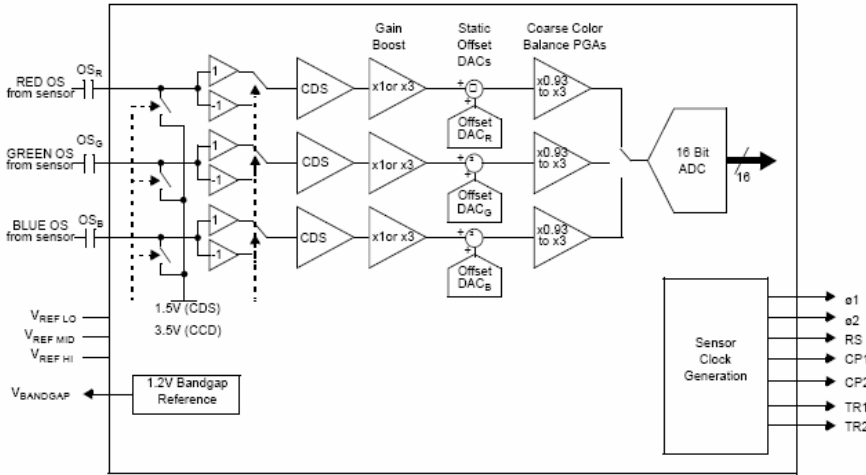
Trigger 2 completes the period trigger, and specifies that the inverse of trigger 1 be used – that is the signal should rise through 400mA on Chan A.

We could have specified a completely independent Trigger 2,

but in many cases, it is faster to let the Cleverscope application work out the inverse of Trigger 1, if we are triggering off the same source.

CCD control

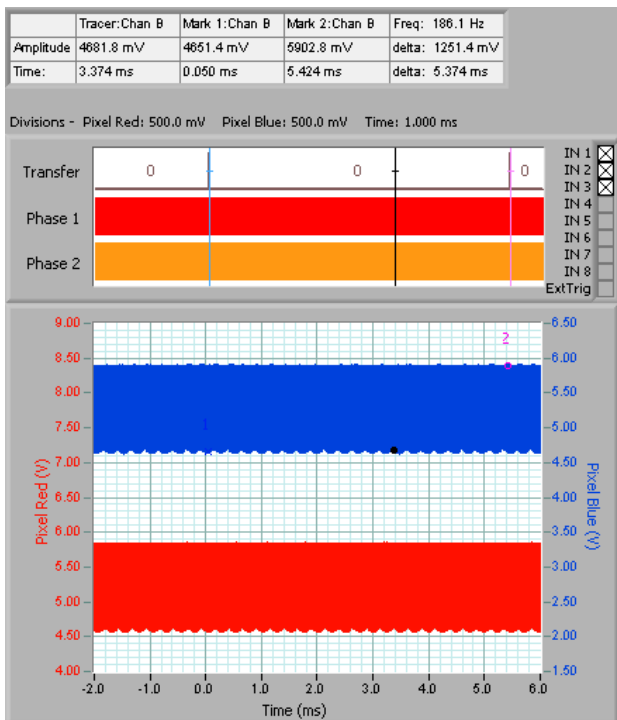
The LM9833 includes a line scan CCD interface, a block diagram is shown below:



The signals $\phi 1$ and $\phi 2$ are the CCD phase clocks, and clock the analog signal through the charge coupled serial register. The signal TR1 (Transfer 1) causes a transfer of the charge from the light sensitive cell to the analog serial register. The CCD includes three analog serial registers – one for each colour. Below we show the big picture – we triggered on the Transfer pulse (see Markers 1 and 2). The update rate is 5.3ms per acquisition, which is the same as the step rate.

Dynamic Range optimised scale and offset

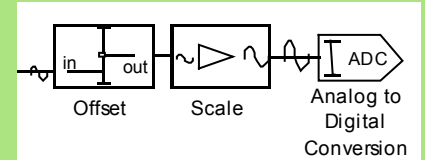
Note that the red and blue CCD voltages are biased in the range 4.5V to 5.8V.



Cleverscope automatically scales and offsets the Cleverscope Acquisition Unit to maximize dynamic range by presenting just the range selected on the scope graph to the Analog to Digital Converter.

Cleverscope dynamic range

Cleverscope always offsets, then scales the input signal so that it fits into the full dynamic range of the Analog to Digital Converter (ADC). This ensures that you make maximum use of the signal information.



As example, to capture the maximum dynamic range, we can set the amplitude axis to a range of 4.5V to 5.8V.

First Cleverscope offsets the input signal from 4.5V to 0V. The -4.5V offset is recorded for display purposes. Next cleverscope scales the 1.3V full scale to 1V full scale (the ADC input range) by reducing the signal $1.3/1 = 1.3$ times. Cleverscope has 26 ranges to ensure that we fit the required dynamic range to an available range. The ADC digitises the input signal with full resolution. This also applies for very small ranges. For example Cleverscope can offset and digitise a 20mV range offset by -20 to +20V.

ADC dynamic range

Cleverscope uses a 10 bit ADC. This means that every measurement is digitised with a resolution of 1 part in 2^{10} , or 1 part in 1024. For our example above, the resolution on the 1.3V scale will be $1300/1024$ which is about 1.27 mV.

Discussion

Scaling and offsetting is exactly what standard oscilloscopes do. However, many of them don't have a very large offset range at the most sensitive scales. Cleverscope has an offset range at least twice as large as a very commonly used oscilloscope.

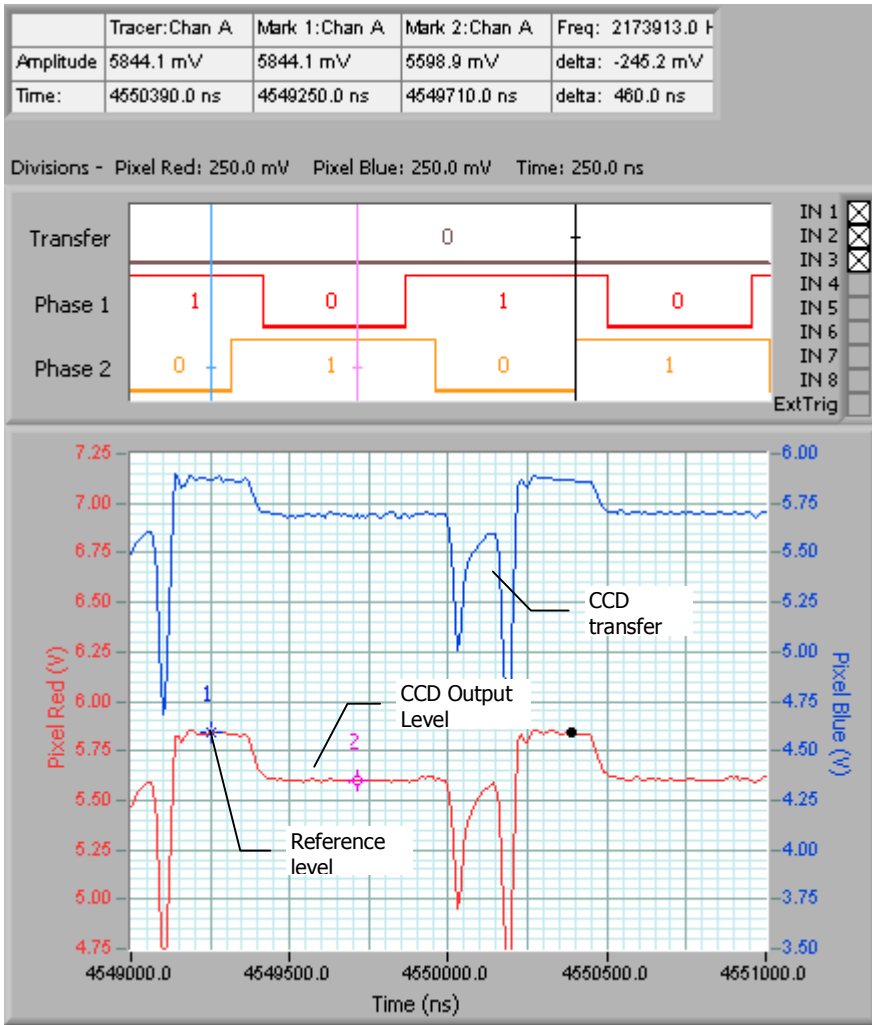
None of the surveyed PC oscilloscopes have offsetting. Instead the ADC just digitises a particular gain setting. For these oscilloscopes to capture a 1.3V signal with a maximum voltage of 5.8V they would have to use a +/-6V range (12V span). Further, most of these scopes are 8 bit, which means they would resolve $12000/256 = 47$ mV, over 37x worse than Cleverscope.

Zooming in, we can see the CCD transfer voltages.

The sequence is as follows:

1. Transfer resets the analog serial register.
2. Phase 1 low enables the CCD register analog output
3. Phase 2 falling initiates transfer to the next register, and output of the reference level.

The CCD converter measures both the reference level and the Output level, and digitizes the difference between these. Here the difference is 245 mV on the Red channel.



Cleverscope Peak Capture

Cleverscope includes the 'Peak Captured' method of signal display. Here you see that the CCD pulses in the CCD transfer region are less than 50ns wide, and yet are correctly shown on the zoomed out graphs. This is because Cleverscope plots both the minimum and maximum amplitude values for all the samples that correspond to a single pixel.

In the previous graph, 8ms of data are displayed. With a display 300 pixels wide, each pixel represents 26.6 us, or 2667 samples. Rather than just showing a single sample to represent the pixel (as some other PC scopes do), Cleverscope examines every sample in the frame (and there maybe two million samples) and for every pixel (in this case 2667 samples) finds the minimum and maximum over those samples, and plots both values as the pixel value. For this reason the earlier graph shows as solid colour.

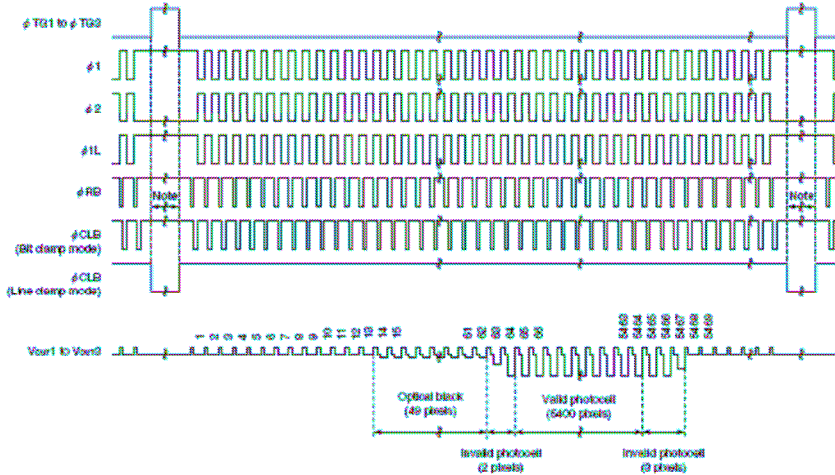
Count based triggering

The CCD outputs pixels continuously. However not all pixels are valid – there is a dummy pixel area following the Transfer pulse, while the CCD is being re-initialised. We would like to bypass this dummy area.

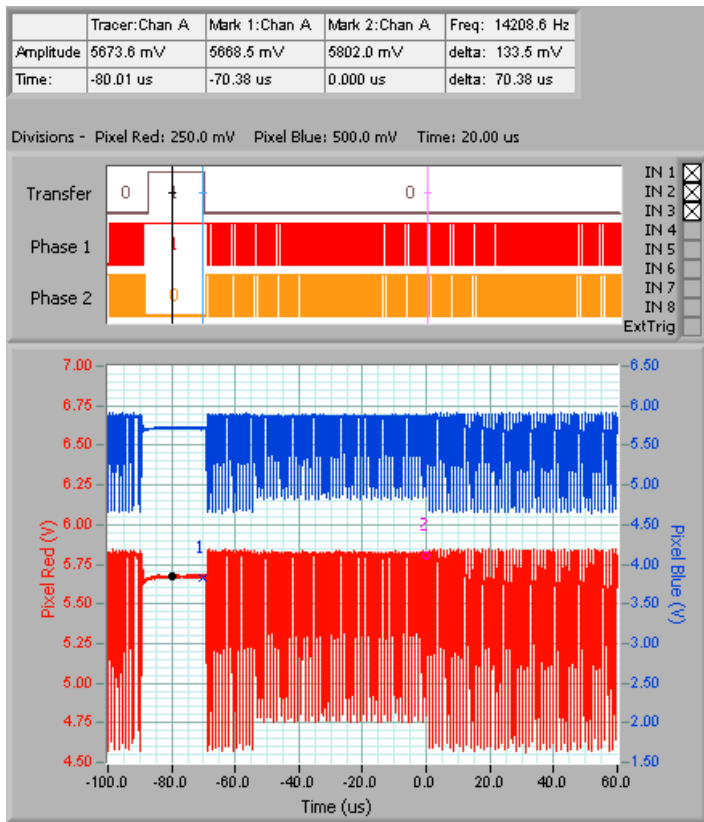
The CCD manufacturer specifies the structure of the pixel output. An example is shown next.

Here is the timing chart for the NEC uPD8861 CCD Sensor used in this design

TIMING CHART 1 (for each color)



The first valid pixel is pixel 65 following the Transfer pulse. We can find this point using the dual trigger – Trigger 1 looks for a falling edge on the Transfer pulse, while Trigger 2 looks for the 65th reference pixel, and sets time 0 to begin there. Here is the output:



As an alternate check that we got it right, we can zoom in some more, and see that the Phase1 clock rate is 1.1us. The total duration to the beginning of the 65th pixel is thus $64 \times 1.1 = 70.4\mu\text{s}$, and this is what we measure.

Finding a particular event

To find the first valid pixel we used a counting trigger.

Trigger 1 detects a falling edge on Digital Input 1, and specifies that Trigger 2 should be counted 65 times to generate a trigger event:

TRIGGER 1 Slope \nearrow

Source \uparrow Dig Trig

Level \uparrow 800m

Holdoff 0

Pre Trigger -100u

Filter \uparrow None

Period Count Trig 2

Trigger min 20n

max 350u

count 65

Digital Pattern **Not Required**

IN 1

IN 2

IN 3

IN 4

IN 5

IN 6

IN 7

IN 8

ExtTrig

Trigger 2 detects a rising edge through 5.75V on Channel A. After the 65th rising edge, a trigger event is generated.

Trigger 2 source Help

Trigger 1 inverted

Trigger 2 definition

Trigger 2 definition

Slope \nearrow

Source \uparrow Chan A

Level \uparrow 5.75

Digital Pattern **Not Required**

IN 1

IN 2

IN 3

IN 4

IN 5

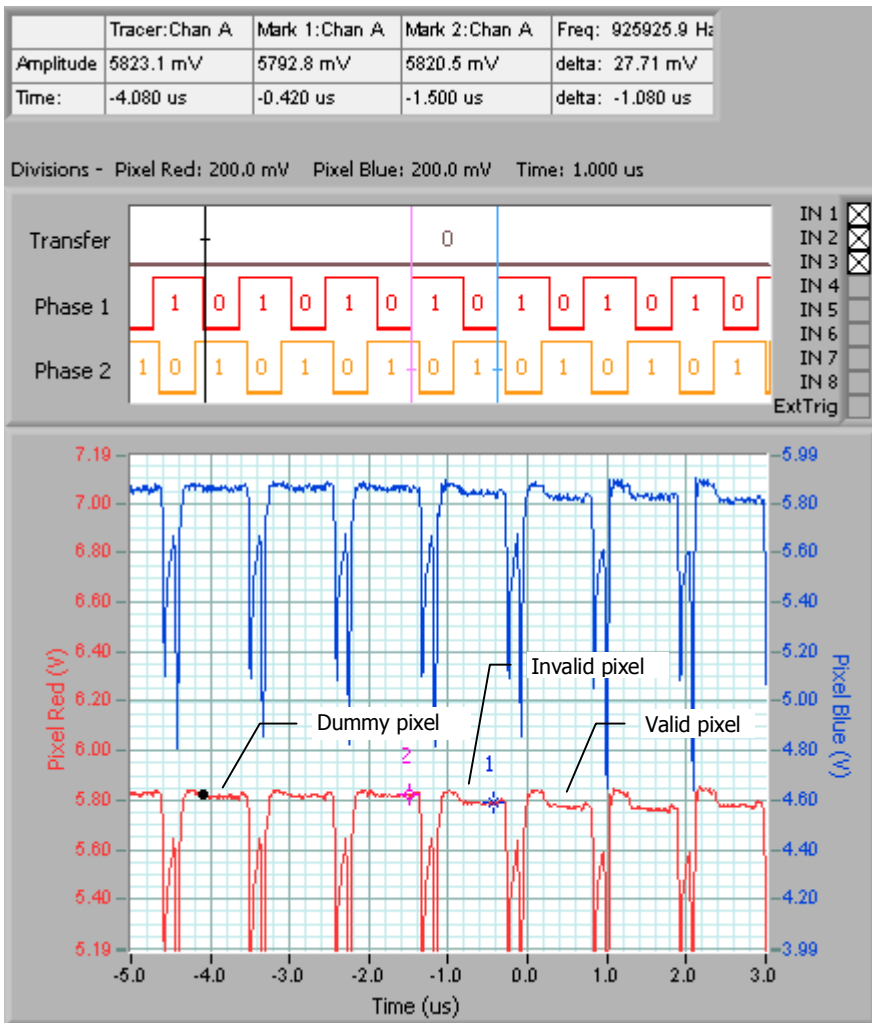
IN 6

IN 7

IN 8

ExtTrig

Here we have zoomed into the 65th pixel.



Digital Graph Formatting

The checkbox control on the right hand side of the digital graph selects the digital inputs to be displayed. As you check/uncheck items, the graph will resize to display only the checked items. The Inputs are displayed in the checked order, meaning that


Transfer = In 1,
Phase 1 = In 2, and
Phase 2 = In 3.

If you have all the digital inputs checked, each individual line is quite small, and you may wish to expand the vertical size of the digital graph. This can be done by selecting Settings/Digital Names and Colours and then setting the Digital Graph Height to Large.

You will note that the digital level for each input is displayed if there is sufficient room. If there is not enough room, just transitions are displayed.


Graph History

As you zoom in or out, you may wish to retrace your steps and go back to a previous view. You can do this for each graph using the history controls

 History is available over the previous 50 changes.


Alignment of graphs

If you manually drag a graph, and then the expand/contract one axis, the division grid lines will become

misaligned. Use the  button to re-align.


Graph View Presets

You can preset the current graph view by using Shift S1 or S2. Then by

clicking on the  buttons, you can restore the preset view.

Annotations

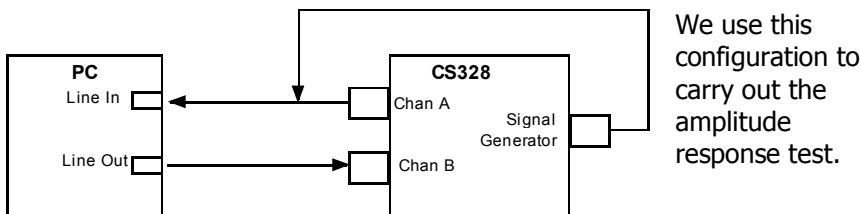
You can annotate the graph by using

the  tool. The annotation is attached to the active, tracked channel.

Filter Response Evaluation

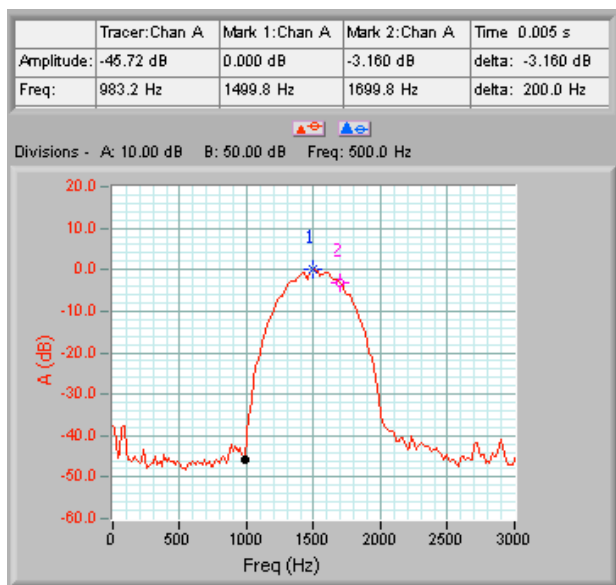
We evaluate the performance of a digital FIR filter, which is part of an under-graduate course on digital filter design. The filter is implemented on a PC, and uses the Sound Card for input and output. The Cleverscope CS328 is used for generation of the stimulus signal – using the built-in signal generator- and for capture of the output signal and display of the spectrum.

In this example the student design filters based on the Finite Impulse Response (FIR) filter structure. Coefficients for the filter were calculated by using the inverse fourier transform to generate the impulse response function brick wall filter characteristic. This will be a sinc ($\sin x/x$) function for an ideal filter. The sinc function is then windowed with a Hanning Window to truncate the impulse to a finite length. Following this the impulse is time scaled to achieve the correct frequency cutoff value, and decimated to generate the coefficients. We examine filters with 50 and 500 taps.



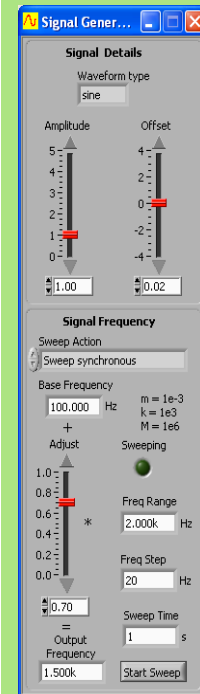
Spectrum Display and Signal Generator Control

Here we plot the amplitude response for a 1500 Hz centre frequency, 500 Hz BW, 50 taps. We start the plot by clicking on the 'Start Sweep' button on the signal generator control.



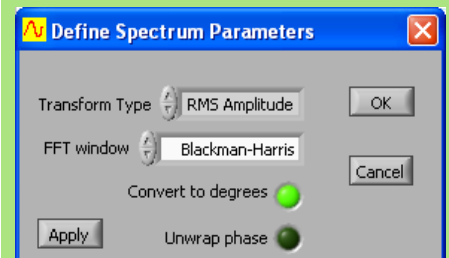
Capturing Frequency Response

The CS328 signal generator is used to output the swept frequency sine wave used to exercise the filter.

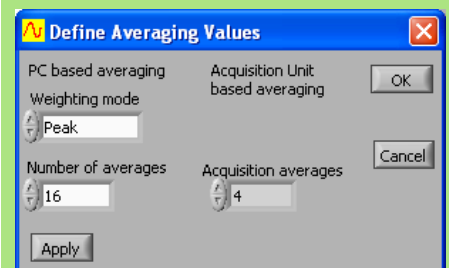


We are testing a 1500 Hz filter, and so we choose a frequency range of 100Hz to 2kHz. This is set using the base frequency and frequency range. We specify sweep synchronous so that the signal frequency is constant for each acquisition to eliminate frequency smearing. The frequency step is 20 Hz to give adequate resolution. The output amplitude is 1V, sine wave with 0 offset.

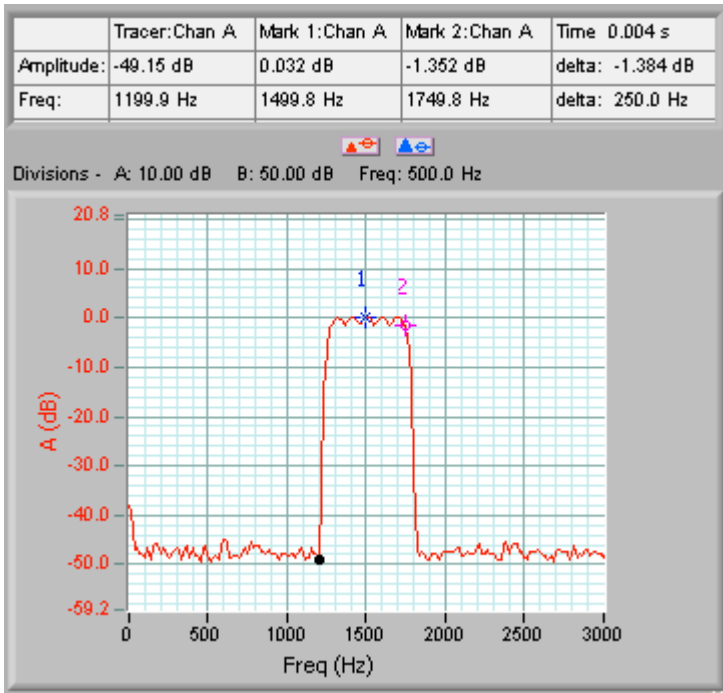
To achieve the amplitude response we choose RMS amplitude as the Transform type.



We specify Peak Averaging. In the frequency domain the spectrum graph accumulates the peak value at each frequency value, building up the frequency amplitude response.



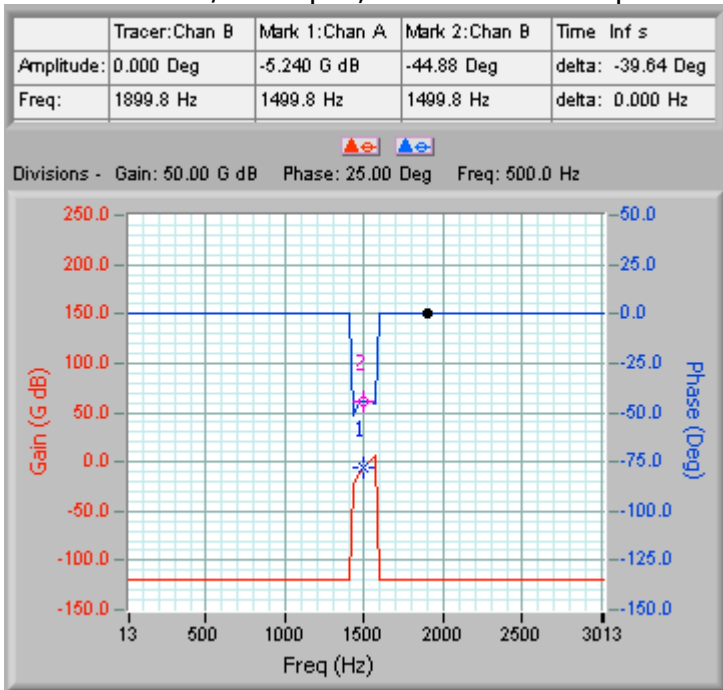
Next we evaluated the filter with 500 taps:



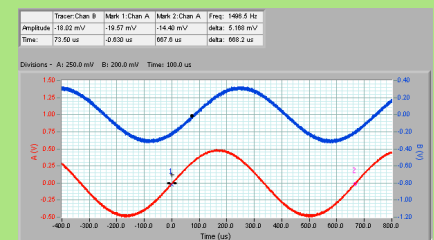
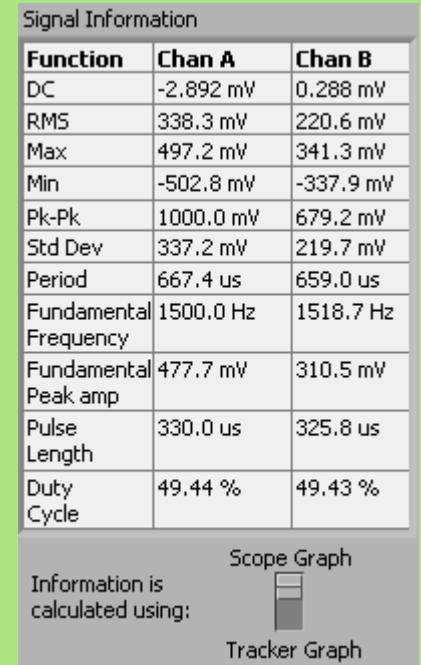
As can be seen, increasing the number of taps increases the fidelity of the filter to the desired brick wall filter. The cost of achieving this is greater processing time, and longer latency.

We can evaluate the phase response of the filter using the Gain/Phase Transform type.

Here is the Gain/Phase plot, for a filter of 50 taps:



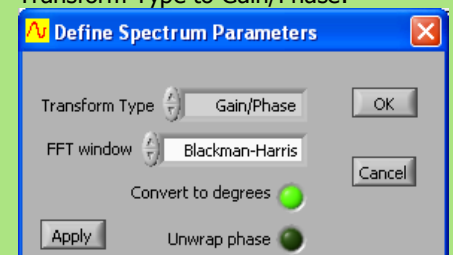
While measuring the filter response we could also check on the signal statistics using the Signal Info in Cleverscope. Here is the signal info for these signals:



Note that at a fixed input frequency of 1500 Hz, the output frequency (on Chan B) was actually 1518 Hz. This indicated that the PC input and output sampling frequencies were not exactly the same, which proved to be the case on further examination!

We can see the effects of the different input and output frequencies in the gain phase plot with a lopsided gain/phase pole at 1500 Hz.

To achieve gain/phase we use settings/spectrum and set the Transform Type to Gain/Phase:



Comparison with other oscilloscopes.

This comparison only looks at key differentiators. Items in **bold** are best values.

Item	Tek TDS2012	Agilent 54622D	Pico 3206	Link Instrument DSO-2102M	Bitscope USB 310	TiePie HS3-100	Cleverscope CS328A	Feature Rank
Analog Input FSD	20 mV – 50V	16 mV – 40V	±100 mV – ±20V	200 mV – 20V	±513mV – ±10.8V	±100 mV – 80V	18 mV – 80V	Important
Analog Channel bit resolution	8	8	8	8	8	8 12 at <50 Msps	10	Important
Analog resolution: hardware coherent averaging	10	10	-	-	-	-	12	Important
Analog Input Offset	±2V: →200mV then ±50V	±25V:→200mV then ±100V	None	±5 divisions	None	None	±3.5V → 200mV then ±80V	Important
Number of digital channels	0	16	0	0	8	0	8	Important
External Trigger	Yes	Yes	Yes – lose sig gen	Yes	No	On extension connector	Yes	Important
External trigger sampled, stored and displayed?	No	No	No	No	No	No	Yes	Useful
Samples of storage, all inputs recorded	2.5k	2000k	500k	32k	64k	128k	4000k	Mandatory
Resolution on 2V offset signal	0.078 mV	0.078 mV	15.6 mV	15.6 mV	15.6 mV	15.6 mV 1mV at <50Msps	0.018 mV	Important
Tracking graph with independent time base	No	No	No	No	No	No	Yes	Important
Dynamic Range (raw unprocessed)	48 dB	48 dB	48 dB	48 dB	48 dB	48 dB 72 dB at <50Msps	60 dB	Important
Sampling Rate, all channels being sampled, MSa/sec	1000	200	100	100	20	100	100	Important
Resolution at 20ms width Width at max sample rate	8 us 2.5us width	20 ns 10 ms width	40 ns 5 ms width	625 ns 320 us width	312 ns 640us width	150 ns 1.3 ms width	10ns 20 ms width	Important
Self Calibration	Yes	Yes	No	No	No	No	Yes	Mandatory
Overload Protection	300 Vrms	300 Vrms	±50V	±150V	±100V	200V	300 Vrms	Mandatory
Separate Earthed BNC for user/PC safety	Yes	Yes	No	?	?	No	Yes	Mandatory
User Units	No	No	Yes	No	No	Yes	Yes	Useful
Glitch resolution	12ns	5ns	None	None	25 ns 1 channel	None	10 ns	Important
Peak Captured to eliminate aliasing	Yes	Yes	No	No	No	No	Yes	Mandatory
Anti-alias filter	Yes – 20 MHz	Yes – 20 MHz	No	No	No	No	Yes, 20 MHz	Useful
Trigger delay	Yes	Yes	No	No	Yes	No	Yes	Useful
Period/ Counting Trigger	No	Yes	No	Yes	No	No	Yes	Important
Dual Independent Triggers	No	No	No	No	No	No	Yes	Important
Mixed signal triggering	No	Yes (no OR)	No	No	State only	Some	Yes	Important

Item	Tek TDS2012	Agilent 54622D	Pico 3206	Link Instruments DSO-2102M	Bitscope USB 310	TiePie HS3-100	Cleverscope CS328A	Feature Rank
USB speed	-	-	12 Mbit/sec	12 Mbit/sec	12 Mbit/sec	480 Mbit/sec	480 Mbit/sec	Useful
Signal Generator	No	No	Yes – lose ext trig	No	Yes – lose Chan B	Yes	Yes	Useful
Sig Gen Range	-	-	100 Hz – 1 MHz	-	100 Hz – 1 Mhz	0.01Hz – 2MHz	0.0.003Hz – 10 MHz	Useful
Voltage Range	-	-	1V fixed sine/tri 5V fixed square	-	?	0- ±12V p-p	0 – 9V p-p	Useful
Voltage Offset	-	-	None	-	None	0- ±12V	±10mV – ±4.5V	Useful
Waveform type	-	-	Sine, square, tri	-	Sine, square, tri, ramp	Sine, square, tri, noise, DC, Arbitrary	Sine, square, triangle	Useful
Spectrum Analysis	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Important
Averaging	Yes	Yes	Yes	Yes	No	Yes	Yes	Mandatory
Mathematical equations	No	No	No	No	No	No	Yes	Important
Math functions	-A, -B, A-B, A+B	-A, -B, A-B, A+B, A*B, integrate, differentiate		-A, -B, A-B, A+B, A*B	-A, -B	-A, -B, A-B, A+B	+ - * / sqrt, log, sin, cos, tan...,integration, differentiation, filtering, multiple equations	Important
User Interface	320 x 240 LCD		Multiple MDI windows all contained in one window	Multiple MDI windows all contained in one window	One window	Multiple separate windows	Dual window with tracking function. Locate anywhere on desktop.	Good one Mandatory
Copy and paste into other document	Possible with extension module, slow		Yes	No	No	Yes	Yes	Mandatory
Subjective view of ease of use	Easy	Easy	Hard	Hard	Hard	Moderate	Easy	Mandatory
Price USD	Scope – 1786 Comms – 390 Total - \$2176	\$5352	\$1456	DSO 2102M USB – 725. Power Supply – 80 Total \$805	B310, no probes \$495 Probes - \$146 Total \$641	\$1207	Scope – 1049 Sig gen plug-in 199 Total - \$1248	Important

Disclaimer: These values are correct to the best of our knowledge on 29 Mar 2006. Cleverscope Ltd accepts no liability for errors or omissions.

We have ranked features Mandatory for the following reasons:

1. If the feature involves safety.
2. If the feature significantly improves versatility in many situations.
3. If the feature provides information that is essential, and can't be acquired any other way.
4. If the feature assures correct performance of the instrument.