Inductance Measurement of Power Chokes

Hubert Kreis

Determining saturation behavior as a function of bias

Interest in power chokes with DC bias is often not so much the initial inductance, but rather the current-dependent changing inductance during operation in the real circuit over the entire operational range up to saturation. But conventional small-signal measuring bridges are out of their depth here!

With the exception of air-core coils, all power inductances show a saturation behavior; their inductance decreases with increasing current. The core materials can lose permeability and then behave like an air core in extreme cases. That saturation behavior limit can be influenced by the choice of core material type, the core geometry, the number of turns, and the air gap.

There are often deviations between the calculated inductance at a certain current (e.g. the nominal current) and the real inductance, perhaps because the choke geometry causes a non-homogeneous field distribution, or the data sheet information of the cores being incomplete. Manufacturing variations of core tolerances are often noticeable, as well as temperature influences. So the saturation behavior of power chokes needs to be measured during product development and also during quality inspection.

Power chokes in Use

Power chokes are required for many applications, e.g. as smoothing chokes for clocked power supplies, as filter chokes for IGBT converters (sine filter), as an impedance for line-commutated converters, as smoothing reactance for circuit blocks and many other circuit needs. One of the main application areas is as a smoothing choke for clocked power supplies (Fig. 1). The voltage curve is for the rectangular choke. The result is a restricted flow of electricity, the one DC component with a superimposed "Strom-Ripple" (Fig. 2). The frequency of this superimposed triangular current corresponds to the clock frequency of the application and can be from a few 100 Hz to a few MHz. For the circuit designer the initial inductance value L0 is usually not of much help. It is the inductance at the highest occurring direct current that is much more important, since it affects the superimposed ripple current (and thus the residual ripple of the power supply) as well as the maximum current through power semiconductors. If the choke effect goes into saturation before reaching the desired maximum output current Iout max, power semiconductors can be damaged or overheated, the capacitor Cout could become overloaded, and the ripple on the output would increase sharply. With most other circuit topologies and many other applications for power chokes (e.g. sinusoidal filters for IGBT converters), the problem is basically the same. With a standard small-signal measuring bridge, only the initial inductance L0 can be measured, since the measurement currents are extremely small. Measuring the saturation behavior requires a corresponding high current to flow through the choke. For the following remarks it is also important to know that the inductance of each choke is frequency-dependant.

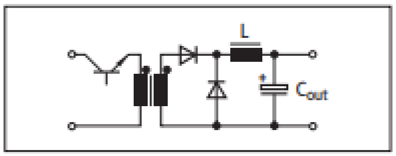

Fig. 1. Typical application of a filter choke, e.g. in clocked power supplies.

Voltage

Current

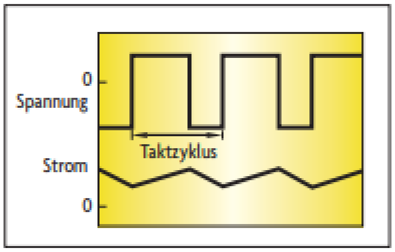

Fig. 2. Typical voltage and current curves for a filter choke.

Clock cycle

Measurement With a Fixed Frequency

There are basically two different inductance measurement methods: the fixed frequency method and the di/dt method. With the fixed frequency method, the test device is fed direct current from a direct current source. A sinusoidal small-signal measurement voltage (e.g. 10 kHz) is superimposed on the current and the inductance is calculated from the amplitude and the phase of the measured current (Fig. 3). The advantage of this method is that the measurement frequency is set precisely and reproducibly. However, the problem with this method is that the measurement conditions have little to do with the real-world application conditions, since the choke does not see a sinusoidal low voltage applied, but rather a rectangular voltage, which has multiple harmonics with it. In addition, a correspondingly powerful direct current source is required, which is available but becomes expensive for larger currents (e.g. over 20 A). To create an inductance curve measurement over the direct current range, it requires many individual measurements be made at different current levels.

Measurement With the di/dt Method

With this method, the test object is subjected to a square-wave voltage pulse as is experienced in the real-world application.

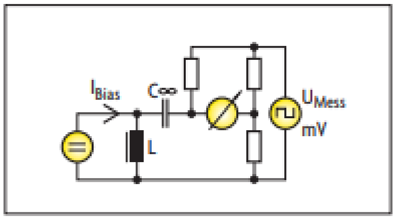

Fig. 3. Fixed Frequency Method measurement setup: The test object is inserted in a measurement bridge and premagnetized from a direct current source. C∞ isolates the component from the measurement bridge.

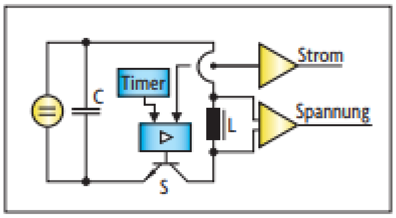

Fig. 4. Measurement setup with the di/dt procedure. The output current is not connected galvanically.

Current is applied to the test item and the current rise di/dt is observed for the inductance and its saturation behavior. When the preset maximum current is reached, the measuring pulse is stopped (Fig. 4). By evaluating the rate of rise di/dt of the measurement current, a complete inductance curve for the test object can be created with a single measurement that shows the inductance curve versus the DC bias. If the voltage of the measurement pulse corresponds to the voltage that is applied to the test object in the real-world application, then the erroneous frequency dependent result of a fixed frequency measurement is eliminated. Another advantage of the pulse-shaped measurement is that the current source does not have to deliver the measurement current continuously and can be be simulated by a capacitor bank. This saves considerable cost and instrument volume.

Figure 5 shows the extended equivalent circuit of the measurement setup. Since the voltage of the measurement pulse at the device under test is never constant due to parasitic voltage drops on the supply lines, the voltage UDUT must be measured directly at the device under test and included in the calculation. The ohmic resistance RL must also be taken into account. However, the influence of CL can almost always be neglected. The following formula then results for $L_L(i) = [U_{DUT}(i) - R_L \times i] \times dt/di$ calculation of the inductance L_L:

Signal Acquisition

Since the di/dt process must work with individual measurement pulses, the current through and the voltage at the test object needs to be recorded and saved for evaluating the resultant curve shape. For good accuracy of inductance, the calculation must use an A/D converter of 12 bit resolution or better, and with a very fast conversion rate (more than 50Msa/s)

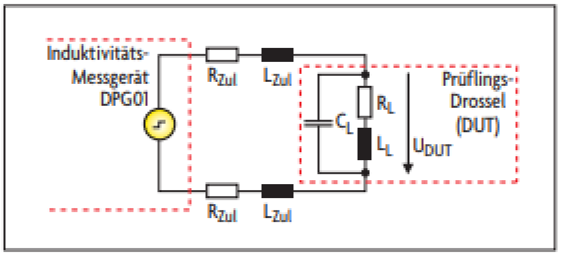

Fig. 5. Extended equivalent circuit of the measuring arrangement for di/dt procedure

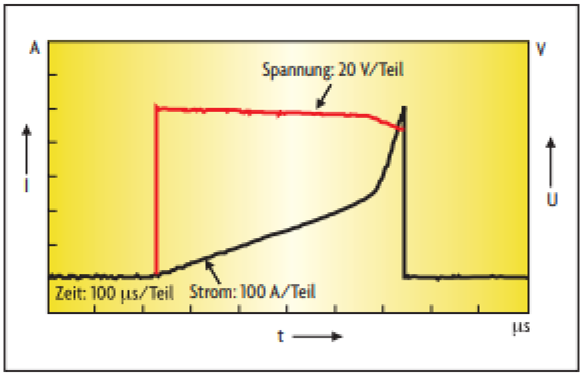

Figure 6. Measured current and voltage curves on a PFC choke with an amorphous cut ribbon core and air gap (LN = 190 µH, IN = 135 A (effective)). The effect goes up at around 200-250 A into saturation.

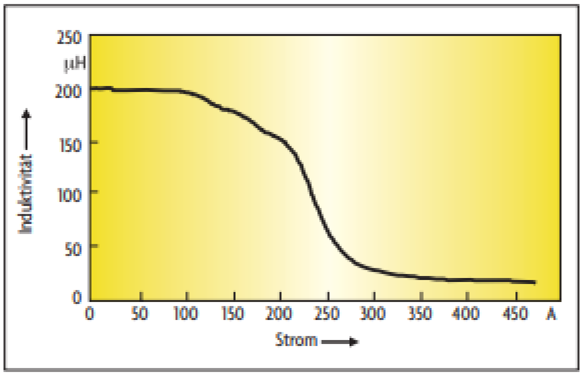

Figure 7. Saturation-dependent inductance curve of the choke in Fig. 6

Figure 6 shows the measurement current and voltage at the test item. In this case it is a PFC choke with an amorphous cut band core and air gap for active power factor correction. The specified nominal inductance L_N is 190µH, the nominal current I_N is 135 A (effective). In this example, the voltage of the measuring pulse is around 100V. When a measurement current of the measuring pulse becomes 500A again completed. Based on the rate of rise of the measuring current, this choke goes into hard saturation at around 200 to 250 A. For ia more precise statement or the creation of an inductance curve, however, a numerical evaluation necessary.

Signal Evaluation

The signal evaluation, i.e. the calculation of the inductance curve, takes place according to the equation above. Increments for Δi or Δt must becarefully chosen. If the step size is too small, even small digitization errors will result in strongly fluctuating inductance curves. With too big a step size, sudden saturation phenomena are not correctly reproduced. What is needed therefore is a dynamic step size control in which the step size automatically adapts dependent on di/dt.

Measurements in Practice

The "Power Choke Tester DPG10 range (see lead photo; manufacturer: www.ed-k.de) uses the di/dt measurement method and has four current ranges for measurement currents from 0.1A to 4000A. This means that the saturation behavior even of very large inductances can be measured. The voltage of the measurement pulse can be set from 10V to 400V. So any inductance can be "supplied" a voltage that is present in the real application (e.g. smoothing a line converter output around 400V, or a smoothing choke with a 5V output, or for an AC/DC converter at around 20V). In addition, the duration of the measurement pulse can be pre-set, which is useful when measuring stress-time areas. The maximum possible pulse energy is limited by the internal capacitor bank supplying the measurement current. At maximum measuring voltage, it is up to 7kJ. This is sufficient even for very large power chokes. In addition, the DPG10 provides automatic measurement and display of ohmic resistance. The operation of the DPG10 and the displayed results is controlled by an attached PC; the measurement protocol features the inductance curve as a function of current as a diagram or in tabular form. Fig. 7 shows the inductance curve of the PFC choke from Fig. 6. This choke at the peak value of the nominal current of 135 A × 1.41 = 190A has an inductance of 156µH. However, the real peak current in the application is reduced due to the superimposed current ripple about 30A. The inductance is then only 127µH, which is 33% below the specified nominal value of 190µH. For the circuit designer this means that the peak current in its application is greater than calculated and thus the selection of the power semiconductors may no longer be sufficient, so that network perturbations and losses increase. From a developer's point of view the choke effect with this saturation behavior is unacceptable.

Dipl.-Ing. Hubert Kreis

Dipl.-Ing. Hubert Kreis was born in Schwäbisch Gmünd and studied electrical engineering at the TU Stuttgart. Since 1994 he has worked for various companies in the development of switching power supplies, electrical drive systems for heavy vehicles and power electronics for aviation equipment. In 2002 he founded the company ed-k, which in addition to customer-specific developments specializes in inductance measuring devices based on the di/dt method.

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