Micsig Optical Isolated Probe For Dynamic Testing of Silicon Carbide (SiC) MOSFETs

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A Silicon Carbide (SiC) MOSFET is a Metal Oxide Semiconductor Field Effect Transistor made with the wide bandgap semiconductor material silicon carbide (SiC). Compared with a traditional silicon (Si) MOSFET, it has a higher breakdown voltage, lower on-resistance, faster switching speed, and better high temperature and high frequency performance.

Case Summary

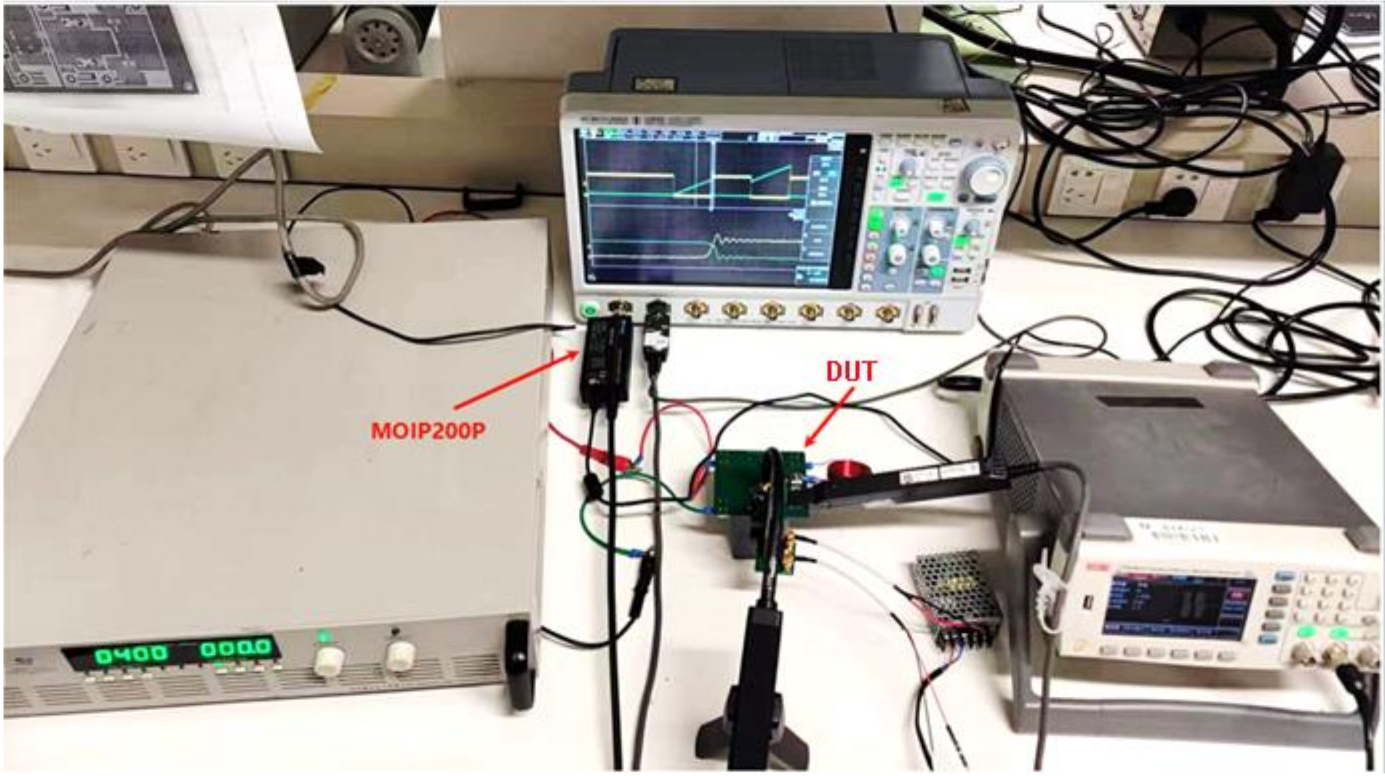
Dynamic testing of SiC MOSFETs can be used to determine key dynamic parameters such as device switching speed and switching loss, helping engineers optimize chip design and packaging. However, due to the extremely fast switching characteristics of SiC MOSFETs, the testing process places higher demands on the parasitic parameters of the measurement system. Factors such as parasitic inductance and capacitance can affect test accuracy and require optimization and control.

Test Example: Device under test: CREE C3M0075120K SiC MOSFET

Test points: SiC MOSFET drain-source voltage and gate voltage

Testing Difficulties

Ordinary passive probes and conventional differential voltage probes have significant parasitic parameters. Due to the extremely fast switching speeds (high dv/dt) of SiC MOSFETs, the probe's parasitic inductance and capacitance can couple with the test circuit, causing significant oscillation or overshoot in the measured voltage signal. Furthermore, the probe's parasitic capacitance can introduce displacement current, causing additional parasitic current to be superimposed on the measured current signal, affecting measurement accuracy.



SiC MOSFET dynamic test platform using the Micsig optical isolated probe MOIP200P

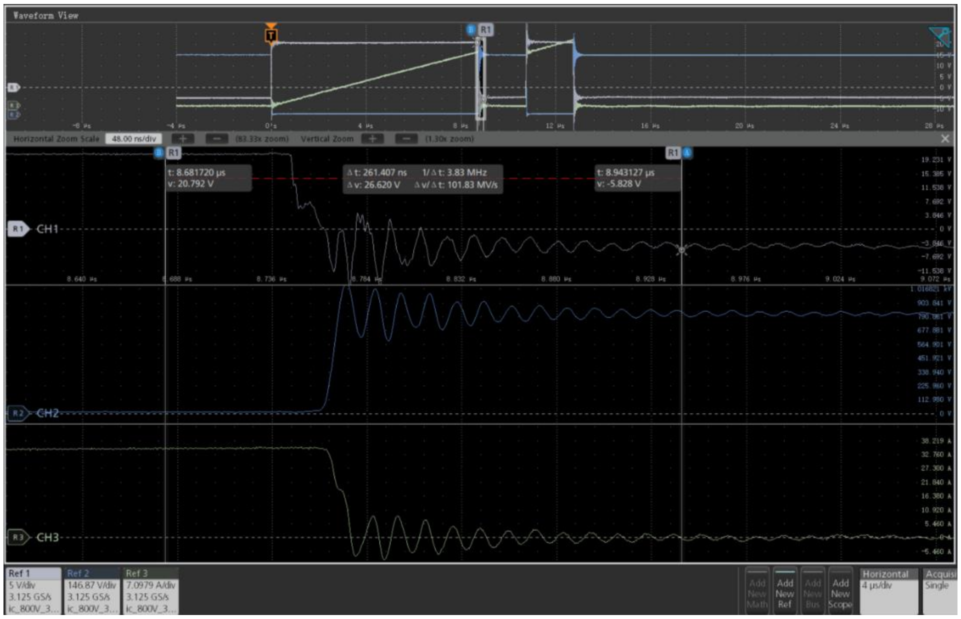
Test effect evaluation

A dynamic test platform was built to evaluate the switching characteristics of SiC MOSFETs. The test platform uses a C3M0075120K SiC MOSFET equipped with a C4D10120A freewheeling diode. The UCC21520 gate driver chip controls the switching of the SiC MOSFET.

To ensure measurement accuracy, drain-source voltage and gate voltage were measured using an optically isolated voltage probe (Micsig MOIP200P). This probe features a 200MHz bandwidth, a high common-mode rejection ratio of 180dB, and a parasitic capacitance of only 1pF, effectively reducing measurement errors. A clamp-on current probe (Hioki 3276) was used for drain-source current, whose 100MHz bandwidth met test requirements. Furthermore, to ensure measurement synchronization, both the voltage and current probes were time-aligned using a calibration circuit.

The waveform in the figure, from top to bottom, shows the gate voltage **Vgs**, drain-source voltage **Vds**, and drain-source current **Ids**. During testing, SiC MOSFETs exhibit extremely fast switching speeds, completing on-off transitions in just over ten nanoseconds. However, electromagnetic interference (EMI) generated during high-speed switching can affect the measurement results.

The optically-isolated probe, with its high common-mode rejection ratio, accurately captures signal details, providing clear, reliable waveform data even in high-noise environments. Furthermore, the optical isolation probe's ultra-low parasitic parameters prevent additional waveform oscillation. The oscillation observed during testing is primarily caused by parasitic inductance in the power circuit and is normal. Comparing the timing relationship between the voltage and current waveforms reveals that the measured switching current contains virtually no additional parasitic current. This is due to the optical isolation probe's low parasitic capacitance of 1pF, significantly reducing measurement error and ensuring the accuracy of the test results.



SiC MOSFET dynamic test results using the Micsig optical isolated probe MOIP200P

Customer Feedback With nanosecond switching dynamic testing of SiC MOSFETs , the probe's 180dB common-mode rejection ratio effectively suppressed high-frequency EMI interference. The measured gate voltage (**Vgs**) and drain-source voltage (**Vds**) waveforms were distortion-free and highly consistent with theoretical simulation results. The 1pF parasitic capacitance negligible additional current error introduced by the measurement system, significantly outperforming traditional differential probes and providing reliable data for switching loss calculations.

Case value summary: Traditional testing pain points: 1. Parasitic parameter interference: The high parasitic capacitance of ordinary differential/passive probes (usually 10~50pF) causes displacement current superposition, destroying the authenticity of the current signal; high parasitic inductance causes voltage oscillation, covering up the true switching waveform.

Common mode interference sensitivity: Traditional probes have low CMRR (typical value <60dB) and are easily affected by high-frequency EMI generated by the high-speed switching of SiC MOSFETs, causing waveform distortion and even tube explosion in severe cases.

Improvements with optical isolation probes:

1. **Low parasitic parameter design:** 1pF parasitic capacitance introduces almost no displacement current, and 180dB CMRR effectively suppresses common-mode noise, ensuring the true capture of nanosecond signals.
2. **Optical transmission anti-interference advantage:** Signals are transmitted through optical fibers, completely isolating ground loop interference and solving the signal distortion problem caused by ground potential differences in traditional probes.

From single-point breakthrough to system innovation The application of optically isolated probes in SiC MOSFET testing not only solves the problem of single-point measurement but also connects the entire process from chip design to packaging to system application through a high-precision data link, becoming a key enabling technology for the upgrade of the wide-band gap semiconductor industry. Their value has transcended the scope of traditional test tools and evolved into industry infrastructure, providing the underlying support for power electronics to move from the "silicon era" to the "silicon carbide era."

Related research: L. Zhang, Z. Zhao, R. Jin, et al, "SiC MOSFET Turn-Off Measurement With Air-Core Inductor Design and RC Snubber Correction," in IEEE Transactions on Instrumentation and Measurement, vol. 74, pp. 1-13, 2025, Art no. 1005013, doi: 10.1109/TIM.2025.3545173.