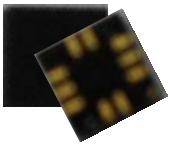
IST8301C
3D Magnetometer Sensor

Datasheet

3-axis Digital Magnetic Sensor

Features



- Single chip 3-axis magnetic sensor
- I2C slave, Fast mode up to 400kHz
- Small font factor: 2.5x2.5x1.0mm, 12-pin BGA
- Heading accuracy of 1 degree
- Wide magnetic field range +/-10 gauss
- Auto zero drift for anti-magnetic interference
- FIFO (32deep) mode for power saving
- Software and algorithm support

Descriptions

The iSentek IST8301C is a 3-axis magnetic sensor. It is an integrated chip with 3-axis magnetic sensors and controller ASIC. IST8301C provides an I2C digital output with fast mode up to 400kHz. The compact form factor is easy to surface mount for high-volume design and production.

Applications

Digital Compass

GPS/pedestrian Navigation

Augmented Reality Applications

Magnetometer

Table of Contents

1 General Description

The iSentek IST8301C is a 3-axis digital magnetometer sensor. It is an integrated chip with 3-axis magnetic sensors and controller ASIC. IST8301C provides an I2C digital output with fast mode up to 400kHz. The compact form factor is easy to surface mount for high-volume design and production.

Features

- Single chip 3-axis magnetic sensor
- I2C slave, Fast mode up to 400kHz
- Small form factor, 2.5x2.5x1.0mm, 12-pin BGA package
- Wide magnetic field range +/- 1000uT
- 13-bit data output
- Auto zero drift for anti magnetic interference
- Low power consumption
- Measurement buffer/FIFO mode for power saving
- Best performance/cost solution

Applications

Digital Compass

GPS/pedestrian Navigation

Augmented Reality Applications

Magnetometer

2 Block Diagram, Package Dimension and Application Circuit

2.1 Block diagram

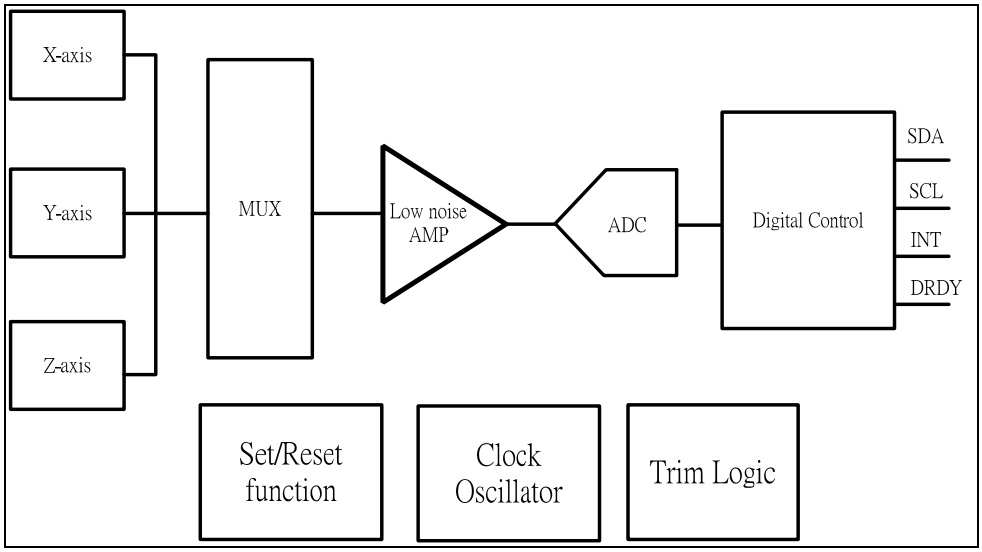
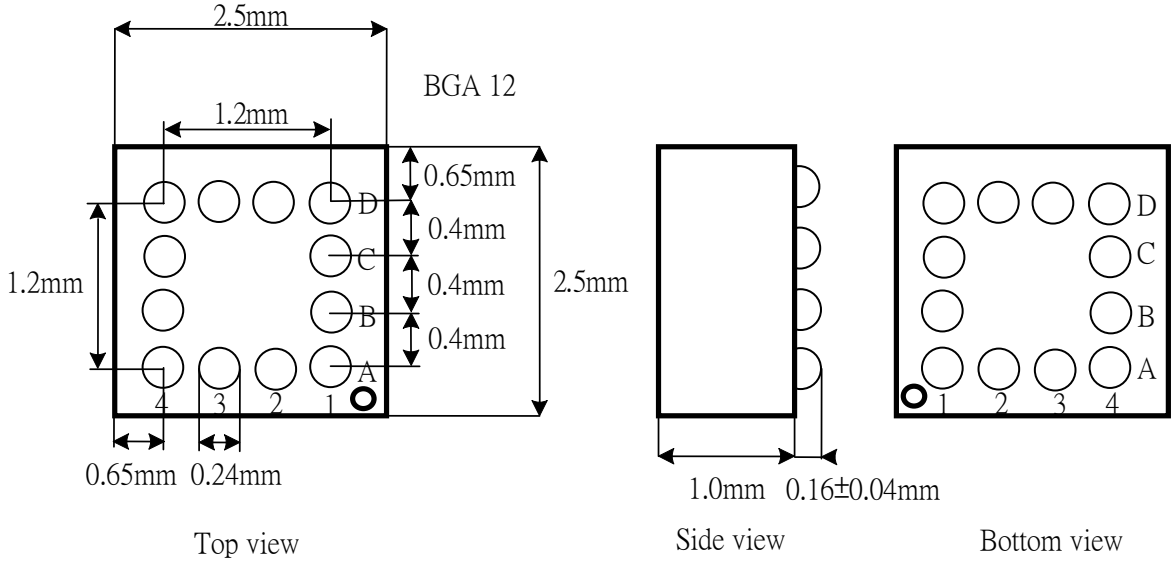
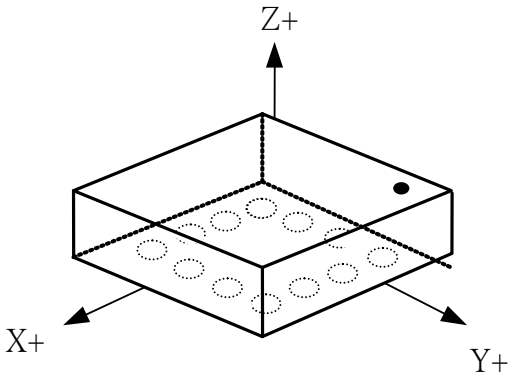


Figure 2-1 Block Diagram

2.2 Package Dimensions and Pin Description

IST8301C dimension and package :





Top view

Pin	Name	Function
A1	DRDY	Data ready
A2	NC	No function
A3	SCL	I2C serial clock
A4	SDA	I2C serial data
B1	AVDD	Regulator input, 2.4~3.6v
B4	VPP	OTP program power
C1	GND	GND
C4	DVDD	Power for I/O, 1.8~AVDD
D1	NC	No function
D2	NC	No function
D3	C1	Set/Reset function
D4	NC	No function

2.3 Application Circuit

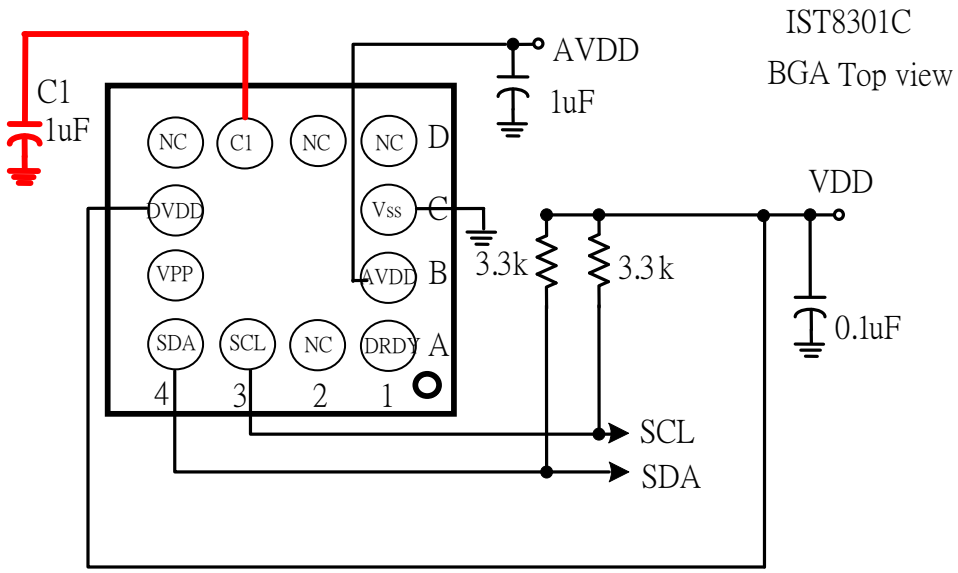


Figure 2-3-1 IST8301C Application circuit

3 Operational Modes and Functional Descriptions

3.1 Three operational modes

3 operational modes for power management are OFF mode, Standby mode and Active mode.

Mode	I2C Bus State	Power Supply		Function Description
		AVDD	DVDD	
OFF	Enabled	OFF	OFF	Not sensor activity
OFF	Enabled	ON	OFF	Not sensor activity, available to accept I2C commands
OFF	Enabled	OFF	ON	Not sensor activity, available to accept I2C commands
Standby	Available	ON	ON	Waiting for active commands Output is available
Active	Available	ON	ON	All functions are available

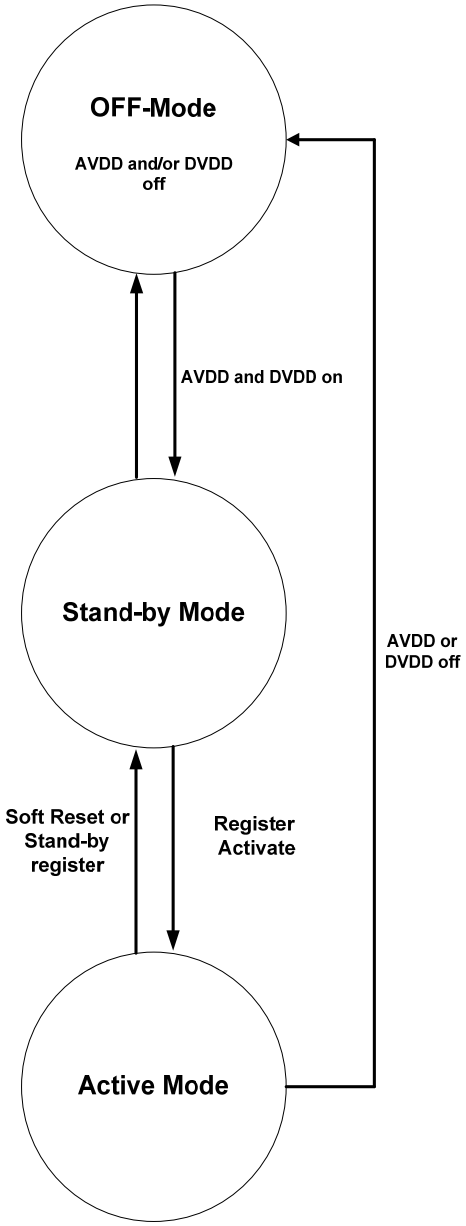


Figure 3-1 3 operational modes and transfer flow.

3.2 Interrupt function

Interrupt function is used for detect the extraordinary external magnetic field occur. When the measured output value is exceeding the threshold, the external pin INT is enabled. Threshold setting is set with the interrupt threshold register (INS)

3.3 DRDY function

DRDY function is used to detect when the output data was updated. The DRDY pin is enabled to notice the data ready output. DRDY is changed to low after reading data in the output register.

3.4 FIFO operation

The IST8301C embeds 32 slots of 16-bit data FIFO for each of three output channel: X, Y, Z. Since the host processor does not need to continuously get data from sensor, FIFO operation allows consistent power saving for system. The FIFO operation can wake up only needed and burst the signification data from the FIFO.
This FIFO operation can work in four different modes: Stream Bypass, FIFO Trigger First, FIFO Trigger Last and FIFO Stream Bypass mode. Each mode is selected by control register CNTL2 (0x1C). Programmable watermark level, FIFO full and FIFO empty events can be enabled to generate dedicated interrupts on the INT pin.

3.5 Stream Bypass mode

In Stream Bypass mode, the FIFO remains empty and does not operate. Only the first address is used for each channel. The remaining FIFO slots are empty.

3.6 FIFO Trigger First mode

When Trigger First happens then the next 32 valid result data sample sets will be stored to FIFO buffer. The coming new measurement data sets are discarded when FIFO gets full. FIFO Trigger First mode waits until interrupt function happens. All new measurement data sets are discarded before trigger.

3.7 FIFO Trigger Last mode

FIFO Trigger Last mode stores data similar to FIFO Trigger Last mode. When interrupt trigger happens, the latest 32 measurement data set is kept in FIFO. The coming new measurement data sets are not stored to FIFO until register FFC bits FF1 and/or FF2 changed or current mode reselected again by host.

3.8 FIFO Stream Bypass mode

FIFO Stream Bypass mode fulfills all FIFO with continuous stream samples or trigger where

only valid new result data sample is stored to FIFO. The oldest measurement data set is discarded and new measurement data is stored to FIFO, after FIFO is full.

4 Electrical Specifications

4.1 Extreme Rating

For E compass

Parameter	Symbol	Limits	Unit
Storage Temperature	TSTG	-40 to +125	°C
Operating Temperature	TOPR	-20 to +85	°C
Regulator Power Input Voltage	AVDD	-0.3 to +4.0	V
I/O Power Voltage	DVDD	-0.3 to +4.0	V
Digital Input Voltage	VIN	-0.3 to DVDD+0.3	V
Electrostatic Discharge Voltage*[1]	VESD	-2000 to 2000	V
Latch Up Current	ALU	-100 to 100	mA

4.2 Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating Temperature	TOPR	-20		+85	°C
Regulator Power Input Voltage	AVDD	2.4		3.60	V
I/O Power Voltage	DVDD	1.65	1.80	3.60	V
Digital Input Voltage	VIN	0		DVDD	V

4.3 Electrical Specifications

(Operating conditions: Ta=+25℃; AVDD=3.0V; VDDIO=1.8V; 1μF ceramic capacitors tied closely to VO and GND respectively.)

Parameter	Symbol	Conditions	Min.	Typ.	Max	Unit
Operating current	IDD3A	Full operation, at 20sps		300		uA
Standby current	ISTB				10	uA

Power down current	IPD	Internal regulator off			2.0	uA
Low pass filter bandwidth	LPF			5		kHz
Output data rate (ODR)	ODR		10		100	Hz
Turn-on time (standby to active mode)				750		us
Turn-on time (active to standby mode)				50		us
Input low voltage	VIL		0		VDDIO *30%	V
Input high voltage	VIH		VDDIO *70%		VDDIO	V
Output low voltage	VOL	IOL= +4mA	0		VDDIO *20%	V
Output high voltage	VOH	IOH= -100uA (Except SCL and SDA)	VDDIO *80%		VDDIO	V

4.4 Magnetic Sensor Specifications

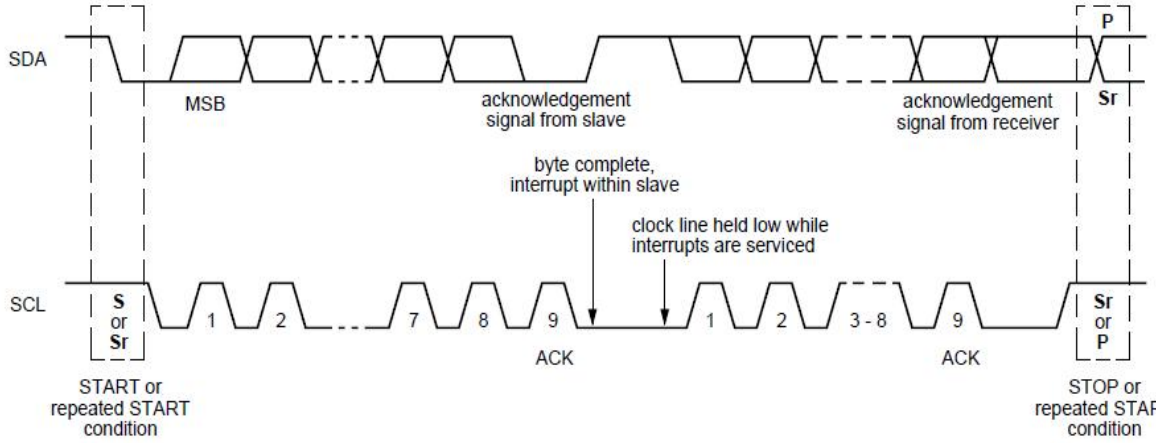
(Operating conditions: Ta=+25℃; AVDD=3.0V; VDDIO=1.8V; 1μF ceramic capacitors tied closely to VO and GND respectively.)

Parameter	Symbol	Conditions	Min.	Typ.	Max	Unit
Dynamic Range	Mdr			±10		gauss
Linearity	Lin	within ±3gauss		1		%FS
Output offset code at zero gauss	Vofs			Vo/2		V
Resolution	Reso			3		milligauss/ bit

5 Digital Interface and Register

5.1 I2C interface

The interface for IST8301C follows the standard I2C definition guidelines with some additional protocol definitions. IST8301C support standard speed (100KHz) and fast speed (400KHz). Pull-up resistors (both in SDA and SCK lines) must be pulled up to 3.3K. The default I2C slave address is 0xE.



5.2 I2C Read Operation

Single Byte Read:

SA	Slave Address+ RW	ACK	Reg Address	ACK	SP	Slave Address+RW	ACK	DATA	NA	ST

Figure 5-2-1 I2C Single Byte Read Operation

ACK: acknowledge, NA: not acknowledge, SA: START Condition, SP: Repeat Start Condition, ST: STOP Condition

■ :Slave to Master □:Master to Slave

Multiple Byte Reads:

SA	Slave Address+ RW	ACK	Reg Address	ACK	SP	Slave Address+RW	ACK	DATA	ACK	DATA	NA	ST

Figure 5-2-2 I2C Multiple Byte Read Operation

ACK: acknowledge, NA: not acknowledge, SA: START Condition, SP: Repeat Start Condition, ST: STOP Condition

■:Slave to Master □:Master to Slave

5.3 I2C Write Operation

Single Byte Write:

SA	Slave Address +RW	ACK	Reg Address	ACK	DATA	ACK	ST

Figure 5-3-1 I2C Single Byte write Operation

ACK: acknowledge, NA: not acknowledge, SA: START Condition, SP: Repeat Start Condition, ST: STOP Condition
■:Slave to Master □:Master to Slave

Multiple Byte Writes:

SA	Slave Address +RW	ACK	Reg Adderss	ACK	DATA	ACK	DATA	NA	ST

Figure 5-3-2 I2C Multiple Byte write Operation

ACK: acknowledge, NA: not acknowledge, SA: START Condition, SP: Repeat Start Condition, ST: STOP Condition
■:Slave to Master □:Master to Slave

5.4 Register

5.4.1 Customer Defined Register

Register name	Typ	I2C Addr	Size (bit)	Info
Output Value x	R	10h	13	Output value of x channel
Output Value y	R	12h	13	Output value of y channel
Output Value z	R	14h	13	Output value of z channel
Status register	R	18h	8	Status of measurement/component
Control setting register 1	R/W	1Bh	8	Component control settings
Control setting register 3	R/W	1Dh	8	Component control settings

Table 5.1 Control/Status Register Map defined by Customer

5.4.2 Output data registers

Output data registers are 13-bit wide for each channel, Data is protected during register read. Data is in 2's complement format and little Endian order. When operating in any FIFO mode,

reading the FIFO output is also through these registers and, the multi-read of register address is burst loop of DATAX, DATAY and DATAZ registers. Host should ignore the bit15 to bit13 when reading these register.

DATAX(0x10)			
Bit	Description	Attr	Default
12:0	X data	R	

DATAY(0x12)			
Bit	Description	Attr	Default
12:0	Y data	R	

DATAZ(0x14)			
Bit	Description	Attr	Default
12:0	Z data	R	

5.4.3 Status register

INS(0x16)			
Bit	Description	Attr	Default
7	Reserved		
6	DRDY: Data ready pin. This status bit is following physical Signal status. Except the polarity signal control. (reference to DRP bit in CNTRL3 register) If data ready is not enabled (reference to DREN bit In CNTL2 register). This bit should be zero. 0 = no Data ready 1= Data is ready	R	0
5	DOR: Output data overrun. If data can not read. This bit Should be set. This bit is released after any output Data register read. 0 =no data overrun. 1= Data is overrun	R	0
4	INT: Combined interrupt information. Set when any of PXSI,PYSI,PZSI,NXSI,NYSI,NZSI	R	0

	Bits is high, reset when reading interrupt latch register (INL) 0= no interrupt event 1= interrupt even happened		
3	FENV: FIFO interrupt event. Set when any of FFU, FEN, WML bits is high Reset when reading interrupt latch register(INL)	R	0
2	FTRG Informs FIFO triggered event occurs in FIFO first And last trigger mode. It will be cleared Automatically when FF1 and FF2 bits of CNTRL2 Register is written.	R/W	0
1	Reserved		
0	Reserved		

5.4.4 Control setting register 1

Controls and adjusts main parameter.

CNTL1(0x1B)			
Bit	Description	Attr	Default
7	PC1: Power Mode Control: 0: Stand-by mode 1: Active mode	R/W	0
6	Reserved		
5	Reserved		
4:3	ODR: Output Data Rate, 2'b00=0.5 SPS 2'b01=10 SPS 2'b10- 20 SPS 2'b11=100 sps	R/W	0
2	Reserved		
1	FS1: Functional state: 0=normal 1=force (default)	R/W	2'b1
0	Reserved		

5.4.5 Control setting register 3

CNTL3(0x1D)			
Bit	Description	Attr	Default
7	SRST : Soft reset, 0=no activity 1=start immediately POR routine -This bit is reset to zero after POR routine	R/W	0
6	FORCE: Starts forced measurement period. 0=no activity 1=start immediately measurement period -This bit is reset to zero after measurement period done - Possible only when force mode selected (CNTL1, bit FS1=1)	R/W	0
5	Reserved		
4	STC : Self-test function challenge set 0=no activity 1=sets AAh to STB egister, when STB register read, set this bit = 0 and also STB =55h	R/W	0
3	Reserved		
2	Reserved		
1	Reserved		
0	Reserved		